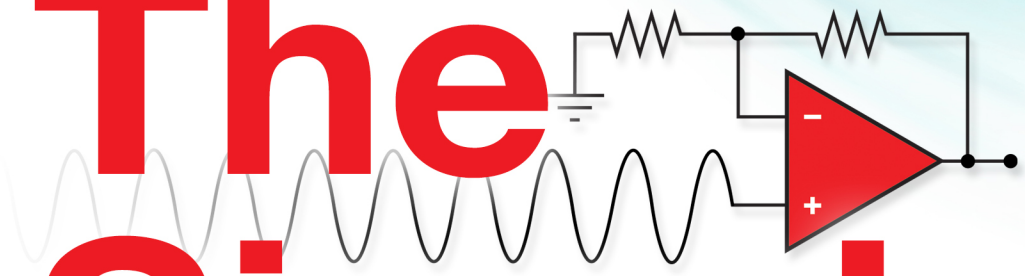
The Signal



A compendium of blog posts on op amp design topics

by Bruce Trump

Texas Instruments

CONTENTS

Preface

I. Op Amp Voltage-Range Issues

1. Op amp voltage ranges: input and output, clearing some confusion
2. Rail-to-rail inputs: what you should know
3. Swinging close to ground: single-supply operation

II. Offset Voltage

4. Offset voltage and open-loop gain: they're cousins
5. SPICEing offset voltage: how to check the sensitivity of circuits to offset voltage
6. Where are the trim pins? Some background on offset-voltage trim pins

III. Input Bias Current

7. "I need high input impedance!" Input impedance vs. input bias current
8. Input bias current of CMOS and JFET amplifiers
9. Temperature effects on input bias current, plus a random quiz
10. Input bias current cancellation resistors: do you really need them?
11. Internal input bias current cancellation of bipolar op amps

IV. Stability and Oscillations

12. Why op amps oscillate: an intuitive look at two frequent causes
13. Taming the oscillating op amp
14. Taming oscillations: the capacitive load problem
15. SPICEing op amp stability
16. Input capacitance: common mode? Differential? Huh?
17. Op amps: G = 1 stable and decompensated
18. The inverting attenuator G = –0.1: is it unstable?

V. Dynamic Behavior

19. Simulating gain bandwidth: the generic op amp model
20. Slew rate: the op amp speed limit
21. Settling time: a look at the character of the settling waveform

VI. Noise

22. Resistor noise: reviewing basics, plus a fun quiz
23. Op amp noise: the noninverting amplifier
24. Op amp noise: but what about the feedback resistors?
25. 1/f noise: the flickering candle
26. Chopper op amps: are they really noisy?

VII. Other Op Amp Issues

27. Bypass capacitors: yes, they are needed, but why?
28. The unused op amp: what to do?
29. Protecting inputs from EOS over-voltage
30. Differential input clamps: can they affect your op amp circuits?
31. Op amps used as comparators: is it okay?

VIII. More Content

32. More content and links

Preface

Learning analog seems like a daunting task. Analog engineers do not generally acquire their experience in a linear path from start to finish: They zigzag a path through an obstacle course of hurdles. They acquire insights in small pieces – a bit here and a bite (not a byte) there. Slowly, puzzle pieces fit into place, and hazy concepts come into focus.

We will never have the satisfaction of jumping a final hurdle or tapping the final puzzle piece into place; that just won't happen. Colleagues much smarter than I am cannot answer all of my questions … and I cannot answer all of yours.

So this assemblage of little analog lessons is hopelessly incomplete. Still, I think you will find it helpful. It may fill some gaps in your knowledge or stimulate your thinking.

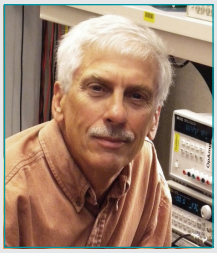
Each topic addressed in this book was originally published as a post on my blog, "The Signal," which you can still visit on TI's E2E™ Community. As such, you'll find that the lessons are short and to the point; practical and intuitive; bite-sized and easy to digest. I needed it to be that way because I'm a simple guy with little patience.

Most of my blog posts sparked questions and other dialogue. I have included links at the end of each topic to the original post when comments were posted. I think you will find some valuable lessons taught there. Furthermore, this compendium does not include all of my blogs. I've included links to other topics, at the end.

If you have any questions about the topics I cover here, or any other precision-amplifier questions for that matter, I hope you will submit them to the Precision Amplifiers forum on TI's E2E Community.

For reference, I created most of the images in this e-book using TI's TINA-TI™ free software tool, downloadable from TI's website.

About the Author



Bruce Trump

As a boy experimenter and ham radio operator, Bruce Trump was drawn to electrical engineering. He never doubted that this was his career path.

After earning a bachelor's degree from Iowa State University, his first industry job took him to Ohio, where he worked on an early laser memory system and other analog system components.

His next stop was at Heath Co. in Michigan designing Heathkits. He tackled a variety of projects there, including electronic clocks, megaphones, metal detectors, navigation calculators and high-power stereo amplifiers.

But hard-core analog was calling him. Burr-Brown, which was a leading provider of analog integrated circuits at that time, offered Bruce an opportunity in Tucson, Arizona, to hang out with and learn from real analog experts.

Texas Instruments acquired Burr-Brown in 2000, marking a new chapter in Bruce's analog career, which included roles in product development, product definition, applications engineering, technical literature, product promotion and business management.

When Bruce reflects on his career, he typically shares that his favorite activity was always dealing with customer application issues.

"I always seemed to work this into whatever role I was currently playing. I particularly enjoyed developing customer seminars and datasheets. It was a challenge to clearly explain the inner workings and applications of precision analog components," he said.

1. Op amp voltage ranges: input and output, clearing some confusion

System designers often have questions about the power supply input and output voltage-range capabilities of operational amplifiers (op amps). It can be confusing, so here is my attempt to sort it out.

First, common op amps do not have ground terminals. A standard op amp does not "know" where ground is, so it cannot know whether it is operating from a dual supply (±) or a single power supply. As long as the power-supply input and output voltages are within their operating ranges, all is well.

Here are three critical voltage ranges to consider:

1. The total supply-voltage range. This is the total voltage between the two supply terminals. For example, ±15 V is a total of 30 V. The operating voltage range for an op amp might be 6 V to 36 V, for example. At the low-voltage extreme, this could be ±3 V or +6 V. At maximum, it could be ±18 V or +36 V or even –6 V/+30 V. Yes, unbalanced supplies are OK, but only if you heed the second and third bullet points below.
2. The input common-mode voltage range (C-M range) is generally specified relative to the positive and negative supply voltages, shown in **Figure 1**. In some equation-like form, the C-M range of this hypothetical op amp would be described as 2 V above the negative rail to 2.5 V below the positive rail. Something like this: (V–)+2 V to (V+)–2.5 V.
3. The output-voltage range (or output-swing capability) is, again, commonly specified relative to the rail voltages. In this case, (V–)+1 V to (V+)–1.5 V.

Figures 1, 2 and **3** show a G = 1 buffer configuration. A key point here: The output capability of the example in **Figure 1** will be limited to 2 V from the negative rail and 2.5 V from the positive rail, which is due to the limited-input C-M range. You would need to configure this op amp in a higher gain to deliver its full output-voltage range.

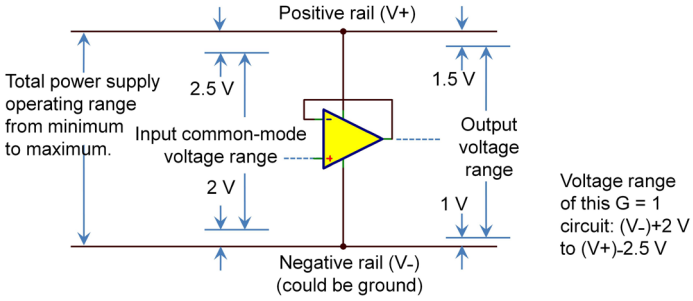


Figure 1: Input and output voltage ranges of a typical op amp used on dual supplies (±).

The example in **Figure 1** is typical of an op amp generally used on dual supplies. It would not be called a "single-supply" type, but it could operate as a single supply by staying within those ranges.

Figure 2 shows a so-called single-supply op amp. It has a C-M range that extends to, and often slightly below, the negative rail. That range allows its use in a wider range of circuits that operate close to ground. So an op amp that is not called "single supply" is actually usable in some single-supply circuits, but a true single-supply type is more versatile.

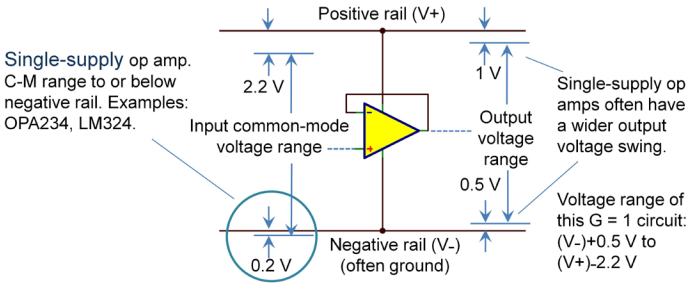


Figure 2: Input and output voltage ranges of a typical single-supply op amp.

In a G = 1 buffer circuit, this op amp could produce an output swing of 0.5 V from the V– rail (limited by the output capability) and 2.2 V from the V+ rail (limited by the input C-M range).

Figure 3 shows a "rail-to-rail" op amp. It can operate with an input voltage equal to or even slightly beyond both supply-voltage rails, as shown in **Figure 3**. A rail-to-rail output means that the output voltage can swing very close to the rails, often within a 10- to 100-mV range from the supply rails. Some op amps claim only a rail-to-rail output, lacking the input characteristics shown in **Figure 3**. Rail-to-rail op amps are very commonly used on single 5-V supplies and lower because they maximize the signal-voltage capability on their limited supply range.

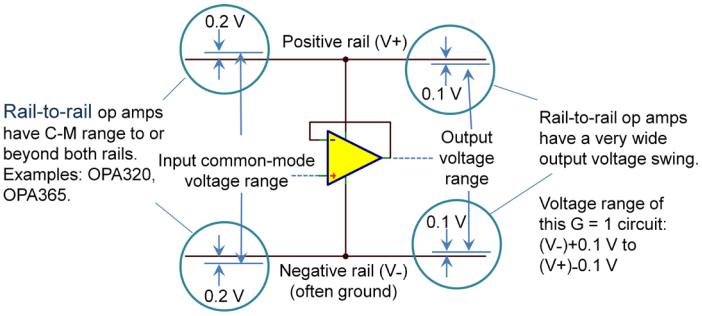


Figure 3: Input and output voltage ranges of a typical rail-to-rail op amp.

Rail-to-rail op amps are appealing because they ease signal-voltage constraints, but they are not always the best choice. Like other life choices, there are often trade-offs with other performance attributes. But that is why you are an analog designer. Your life is full of complex issues and trade-offs, and you love it!

To see this original post with comments, click here.

2. Rail-to-rail inputs: what you should know!

Rail-to-rail operational amplifiers (op amps) are extremely popular and especially useful with low supply voltages. You should know how to accomplish rail-to-rail inputs and understand some trade-offs.

Figure 4 shows a typical dual-input, rail-to-rail stage comprising both N-channel and P-channel transistor pairs. P-channel field-effect transistors (FETs) handle the signal through the lower portion of the common-mode voltage range to slightly below the negative rail (or single-supply ground).

The N-channel FETs operate with a common-mode voltage near and slightly above the positive rail. Additional circuitry (not shown) directs traffic, determining which input-stage signal the next stage will process. Most TI dual-input-stage op amps are designed so that the transition occurs approximately 1.3 V from the positive rail. Above this voltage, there is insufficient gate voltage for the P-channel stage, so the signal path is redirected to the N-channel stage.

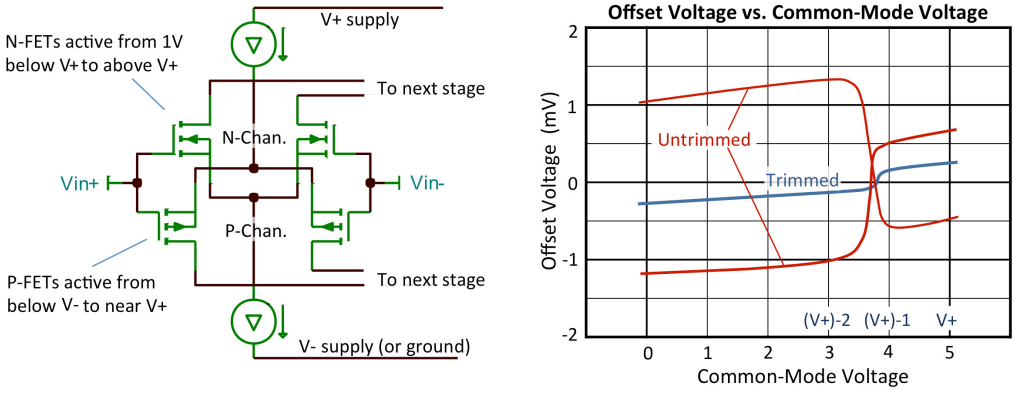


Figure 4: A typical dual-input rail-to-rail stage using both N- and P-channel transistor pairs.

The P and N input stages will have somewhat different offset voltages. If the common-mode voltage moves through this transition (as it does with rail-to-rail G = 1 operation), it creates a change in the offset. Some op amps are factory-trimmed by laser or electronic trimming, adjusted to reduce the offset of the input stages. This trimming reduces the change through the transition but still leaves a residual bobble. Circuitry controlling the transition from the P to N input stage is referenced to the positive supply voltage, not to ground. On a 3.3-V supply, the transition moves to an awkward point – midsupply.

While unnoticed in most applications, this change in offset voltage may be an issue if you require high accuracy. It can also cause distortion in alternating current (AC) applications. But again, distortion will only occur if the common-mode input voltage crosses the transition between stages.

Figure 5 shows a second type of rail-to-rail input stage. An internal charge pump boosts the voltage powering a single P-channel input stage to approximately 2 V above the positive supply rail. This voltage boost allows a single-input stage to perform seamlessly over the full rail-to-rail input-voltage range – below the bottom rail to above the top rail – with no transition glitch.

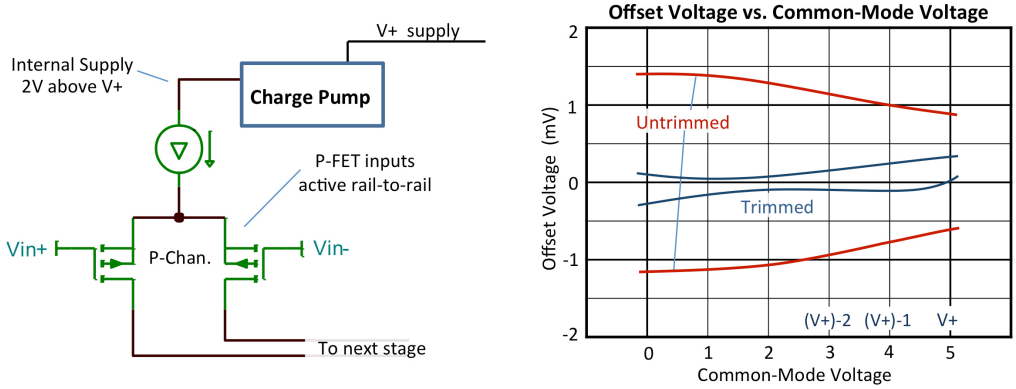


Figure 5: A rail-to-rail input stage with an internal charge pump to boost the voltage, powering a single P-channel FET.

"Charge pump" ... it sounds spooky to some designers. They are noisy, right? But TI's most recent ones are remarkably quiet. Charge pumps require very little current because they only power the input stage. There are no extra pins or capacitors – it is all internal. Charge-pump noise is below the broadband noise level; rarely can you see it in the time domain. Applications that analyze the spectral response below the broadband noise level, however, may see some artifacts.

Not all applications need an op amp with rail-to-rail input. Inverting op amp circuits or amplifiers in gain greater than unity, for example, often do not require rail-to-rail input, yet still have rail-to-rail output. Do you really need a rail-to-rail input amplifier? Many engineers prefer to use them so that they do not need to worry about exceeding the common-mode range. They use the same op amp in various points in their systems: some need rail-to-rail input; others not. Whatever your choice, with knowledge of rail-to-rail types and trade-offs, you can select more wisely. If in doubt, you are welcome to ask the engineers on the TI E2E™ Community Precision Amplifiers forum.

Here are a few example op amps:

- OPA340 dual-input stage, trimmed offset, 5.5-MHz, rail-to-rail CMOS.
- OPA343 dual-input stage, untrimmed offset, 5.5-MHz, rail-to-rail CMOS.
- OPA320 charge-pumped input stage, 20 MHz, rail-to-rail CMOS.
- OPA322 charge-pumped input stage, untrimmed offset, 20 MHz, rail-to-rail CMOS.

To see this original post with comments, click here.

3. Swinging close to ground: single-supply operation

Rail-to-rail amplifiers can produce output voltages very close to ground – but how close? I am talking about complementary metal-oxide semiconductor (CMOS) operational amplifiers (op amps) that often are used in low-voltage designs when you are trying to maximize output-voltage swing. TI's specifications for these devices generally look something like **Table 1**.

Parameter	Conditions	Min	Typ	Max	Unit
Output					
Voltage output swing from both rails	RL = 10 kΩ		15	25	mV
	RL = 2 kΩ		35	50	mV

Table 1: Output specifications for rail-to-rail amplifiers.

Table 1 makes it appear that the output will never swing much closer than 15 mV from ground, and that last 15 mV can be critical for accurate zero-based measurements. But wait: You really need to carefully interpret all of the conditions of this specification, because the assumption is that the load is connected halfway between the power-supply terminals.

You will often find conditions cited at the top of the specifications table, where you will see a statement like this: R_L connected to $V_S/2$.

In this specified condition, the amplifier must sink current through the load resistor as the output approaches ground. This reflects the way the amplifier is tested, assuring that it can properly source and sink current. It is a sensible and conservative way to test and specify the amplifier, but what if it is not the way your load is connected? Suppose your load is connected to ground as in **Figure 6**. The load resistor actually helps pull the output to ground, and the amplifier is not required to sink current.

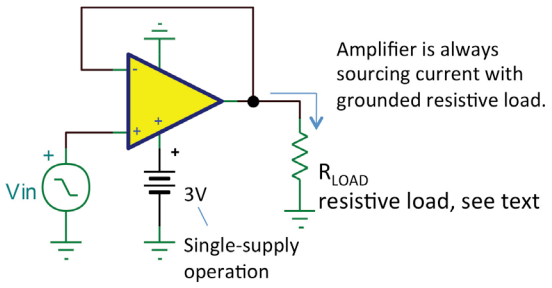
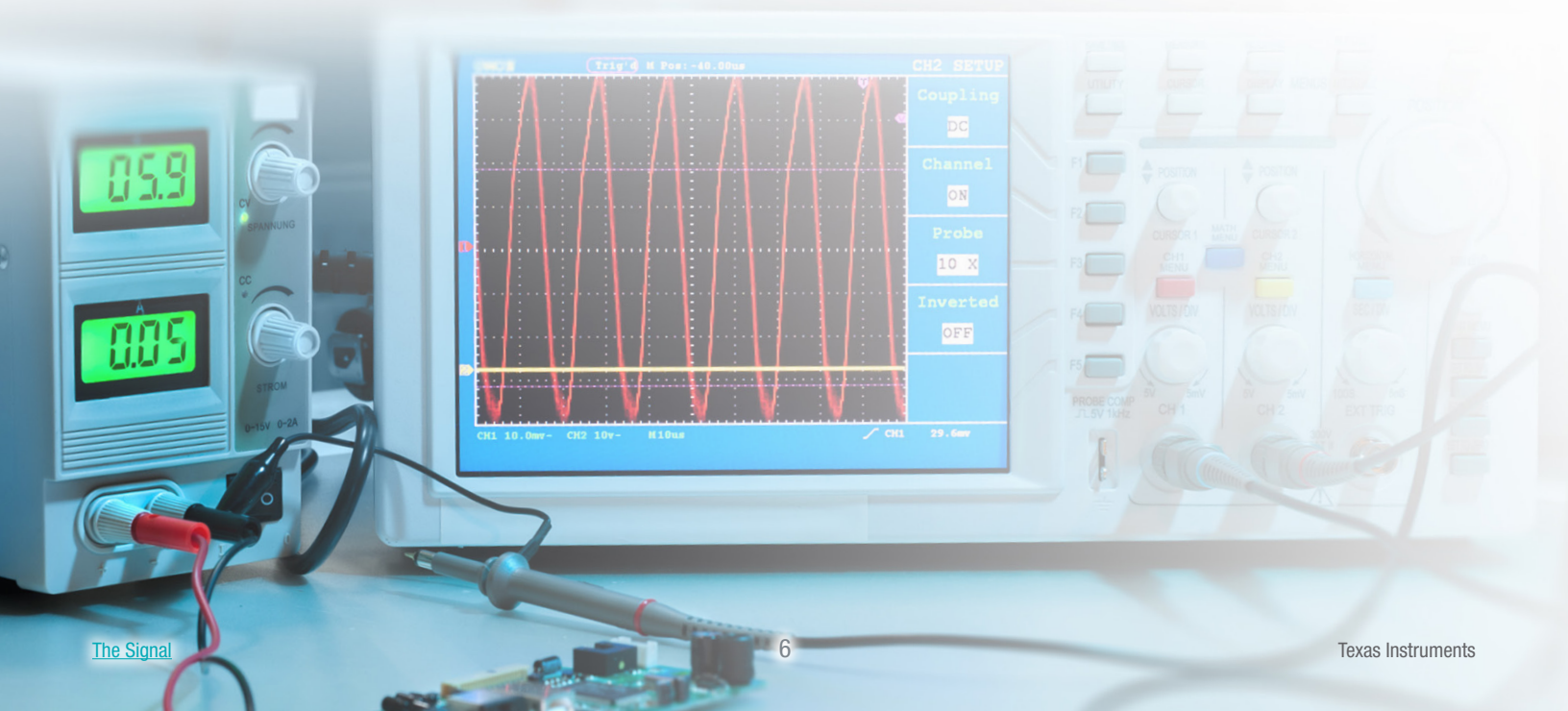


Figure 6: Example of an amplifier load connected to ground.



In this condition, most CMOS op amps can swing very close to ground – within a millivolt or two. The specifications may not highlight this capability, but it is hinted at in **Figure 7**, showing output-voltage swing as a function of output current. The graph could perhaps benefit from more resolution, but you can see that the output voltage converging on the specified voltage rails for this test is ±2.75 V. For single-supply operation, the V– supply is equal to 0 V.

Now I need to add a few provisions. Notice that in **Figure 8**, the feedback network is referenced to ground. You need to consider all sources of load on the amplifier, not just RL. In this case, R1 + R2 are effectively additional ground-referenced loads in parallel to RL. But if R1 is referenced to a positive voltage, the amplifier would have to sink current coming through the feedback network as the output neared 0 V. The output would not be able to swing quite so close to ground.

In this same circuit, if the gain is high, the input offset voltage may affect your apparent output swing. For example, in G = 20, if the input offset voltage of the op amp is +1 mV, zero input will produce a 20-mV output. That is not due to an output-swing limitation – it is an offset-voltage issue. Of course, a small, negative input voltage will bring the output very near 0 V, but your circuit may never have a negative input voltage.

Alternating current (AC) signals with reactive loads may be an exception. Load current and voltage are not in phase with a reactive load, so the amplifier may have to sink current as the output voltage approaches ground.

(Referring to CMOS op amps, bipolar op amps cannot swing so close to ground.)

Low-voltage battery-operated circuits are challenging, and it seems that we are always struggling to maximize voltage swings. With a good understanding of op amp capabilities, you may be able to squeak out additional output swing close to ground. If you have questions about a specific amplifier or circuit configuration, submit your question to the Precision Amplifiers forum on TI's E2E Community.

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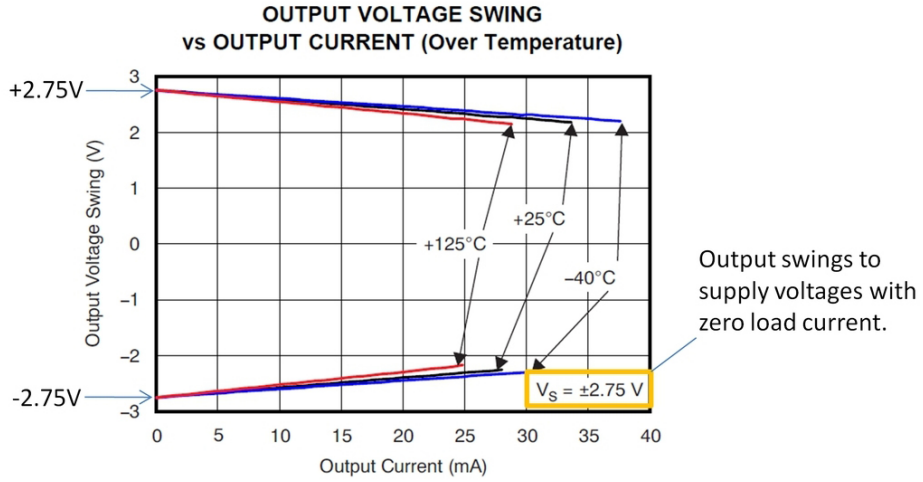

Figure 7: Output-voltage swing shown as a function of output current.

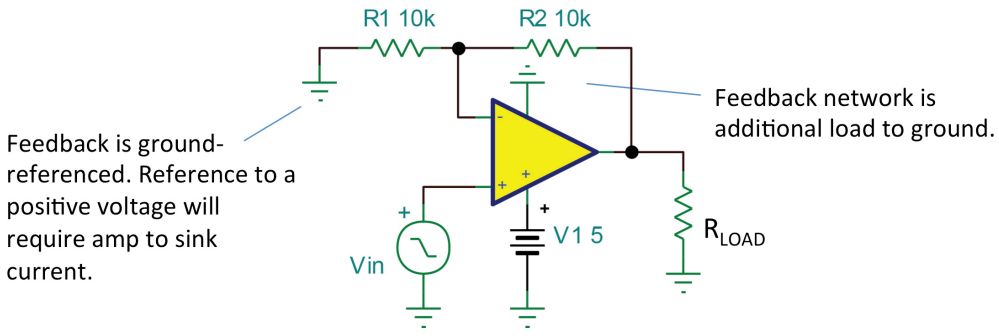

Figure 8: Single-supply op amp configuration with the feedback network referenced to ground.

4. Offset voltage and open-loop gain: they are cousins

Everyone knows what offset voltage is, right? In the simplest G = 1 circuit of **Figure 9a**, the output voltage is the offset voltage of the operational amplifier (op amp). The offset voltage is modeled as a direct current (DC) voltage in series with one input terminal. In unity gain, the offset is passed directly to the output with G = 1. In the high-gain circuit (**Figure 9b**), the output voltage is 1000 Vos. Right?

Well, nearly so, but not quite. Understanding the "not quite" can help you understand errors in your op amp circuits.

In the first case, the output voltage was very near midsupply (assuming dual supplies). This is the output voltage at which TI defines and tests offset voltage. But in the second case, the output may be several volts, assuming several millivolts of offset. That requires a small additional differential voltage at the input of the op amp to create the output swing (according to the open-loop gain of that particular amplifier).

Let us run some numbers. "If the DC open-loop gain is 100 dB, that amounts to 1/10^(100 dB/20) = 10 µV/V. So for every volt of output swing from midsupply, the input voltage must change by 10 µV. Think of it as an offset voltage that changes with the DC output voltage. With 9 V of output swing, that is a 90-µV change. Maybe that is insignificant in your circuits, maybe not.

The point is that thinking of finite open-loop gain as a changing offset voltage with a change in output voltage provides an intuitive way to size up the error. And the character of that error may matter, too. To test offset voltage and open-loop gain, use a fancy two-amp loop circuit. With it, you can control the output voltage and measure the offset voltage. If you sweep the output voltage through its full output range, the change in offset voltage often looks something like **Figure 10**.

Note that the greatest change in offset voltage tends to occur at the output extremes, near the positive and negative rail. The op amp is "straining" to produce its maximum output. The incremental open-loop gain is higher in the middle and falls where the output nears the rails. As you plan your circuits, expect that this will be the case. Offset voltage will increase more dramatically as you push the op amp to its swing limits.

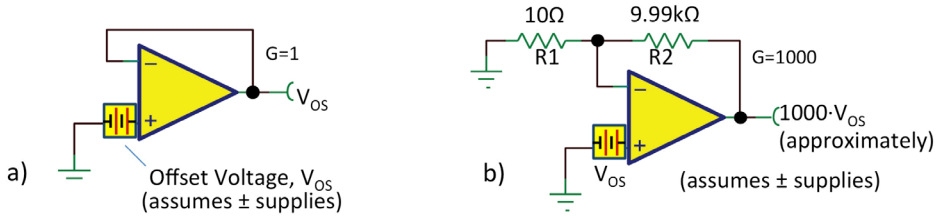

Figure 9: Output offset voltage where G = 1 V/V (a) and G = 1,000 V/V (b).

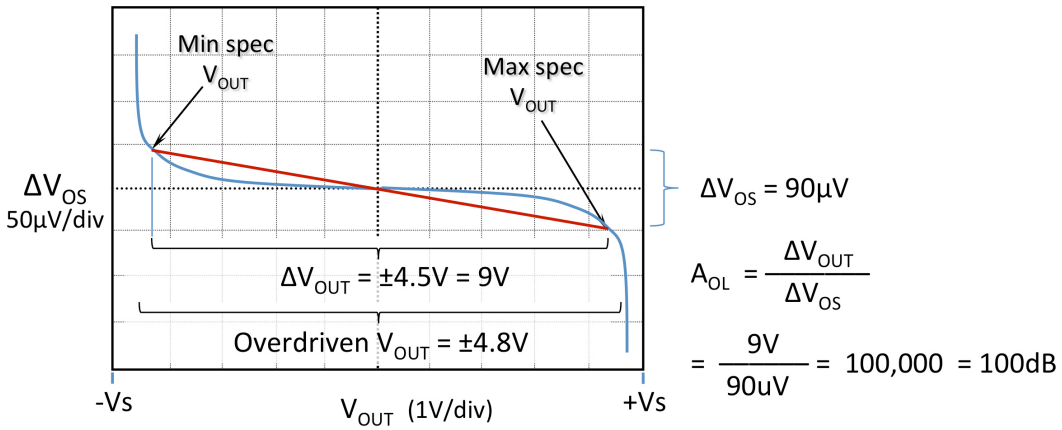

Figure 10: Offset-voltage change shown as a function of output voltage.

Not all op amp manufacturers specify A_{OL} the same way. TI tests its precision op amps for open-loop gain, which is averaged over a generous output-swing range for good linear operation (the red line in **Figure 10**). In the specifications table, it looks like **Table 2**.

When the amplifier is overdriven (creating a larger offset voltage), the output will swing closer to the rails. Sometimes output swing differs from the conditions in **Table 2**. The output swing in **Table 3**, for example, shows the output voltage with the input overdriven. My op amp development group at TI affectionately called this a "slam spec," meaning that the input is overdriven and slammed as far as it can go to the rail.

Both types of specs are useful, depending on the requirements of your application. The key is to understand and carefully interpret the specifications.

To see this original post with comments, click here.

Open-Loop Gain	Conditions	Min	Typ	Max	Unit
Open-loop gain A_{OL}	(V-) + 0.5 V < V_O < (V+) - 0.5 V, R_L = 10 kΩ	100	120	–	dB
	(V-) + 0.5 V < V_O < (V+) - 0.5 V, R_L = 2 KΩ	96	116	–	dB

Minimum A_{OL} is assured with an output swing 0.5 V from rails.

Two load conditions shown. Higher A_{OL} with 10 k load.

Table 2: Open-loop gain specifications shown with different loads and output voltage swings.

Output	Conditions	Min	Typ	Max	Unit
Voltage output swing from rails	R_L = 10 kΩ	0.2	0.15	–	V
	R_L = 2 kΩ	0.3	0.2	–	V

Table 3: Example of an output voltage swing with the input overdriven.

5. SPICEing offset voltage: how to check the sensitivity of circuits to offset voltage

It may not always be obvious how offset voltage will affect a circuit. "Direct current (DC) offsets are easy to simulate with a simulation program with integrated circuit emphasis (SPICE), but operational amplifier (op amp) macromodels only predict the effects of offset voltage of one unit. What about variation from device to device?

The improved Howland current-source circuit (**Figure 11**) provides a good example. Its feedback to both input terminals may leave you wondering how the input offset voltage (V_{OS}) of the op amp contributes to error. The OPA548 is a hefty power op amp with a 5-A maximum output and 60-V supply capability. It is frequently used in Howland circuits. But how will its 10-mV maximum offset voltage affect the output current of the circuit?

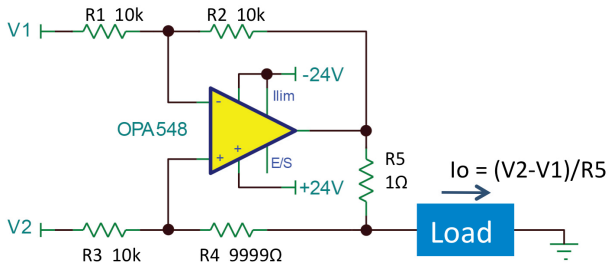

Figure 11: An example circuit—an improved Howland current source.

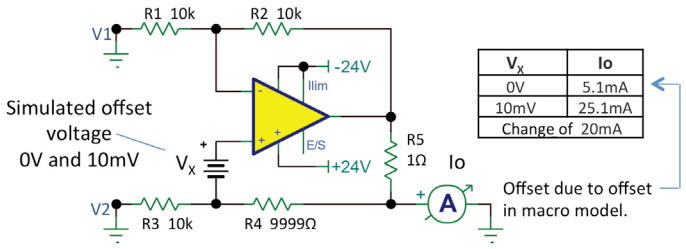

Figure 12: Output offset current due to op amp offset-voltage in an improved Howland current source.

Before simulating, this is an opportunity to exercise best practices with SPICE. What do you think the output current will be with 10 mV of input offset voltage?

Offset voltage is modeled as a voltage source in series with one of the input terminals. So in SPICE, you can merely insert a DC source in series with one of the inputs to induce the effect of varying offset voltage. With V1 and V2 inputs connected to ground, ideally you would expect zero output current. But the offset voltage will supply a small input: a DC simulation with V_X = 0 and V_X = 10 mV. Note the change in output current due to the change in V_X (**Figure 12**). There may be other sources of offset, so the delta in output current from these two V_X values reveals the contribution of offset voltage. Of course, the offset could also be negative.

The output offset with V_X = 0 in the simulation comes from the offset voltage (2.56 mV) included in the OPA548 macromodel – and would not be an additional contributor. Most of TI's macromodels have an offset voltage approximately equal to the typical offset voltage value. In some circuits, other sources of output offsets could come from input bias current and/or input offset current and would be additional contributors to total offset.

What output offset current did you predict? The improved Howland is essentially a difference amplifier (four resistors around an op amp) with an added resistor, R5. This unity-gain difference amplifier (equal resistors) causes the input difference voltage (V2-V1) to be impressed on R5; the resulting current flows to the load. The offset voltage, however, is applied directly to the noninverting input and is amplified by +2 – like a noninverting amplifier (G = 1 + R2/R1). Thus, a 10-mV offset voltage creates 20 mV across R5, producing a 20-mA output current offset. A -10-mV offset would create a -20-mA output current (current sinking from the load).

Maybe you see it intuitively, maybe you don't. Either way, SPICE can provide confirmation.

To see this original post with comments, click here.

6. Where are the trim pins? Some background on offset-voltage trim pins

In 2012, my colleague Soufiane Bendaoud published an article, "Pushing the Precision Envelope." In it, he discussed various technologies that TI uses to "trim" or adjust the offset voltage of its amplifiers to very low values. It got me thinking about offset voltage trim pins. Where do they go?

Newer operational amplifiers (op amps) lack the offset voltage trim pins once found on virtually all op amps. There are many factors at work in this change. Better, lower-offset amplifiers, autocalibrated system designs, pressure to reduce assembly and adjustment costs, tiny surface-mount packages – all combine to reduce the use of offset trim pins. Still, many of our best-selling op amps have trim pins, and knowledge and best practices of how to use (or not use) them are fading.

This much is easy: if you do not use the trim pins, leave them open circuit, with no connection. Do not connect them to ground.

Figure 13 shows a common type of internal trim circuitry. Trim pins connect to a tapped portion of the input-stage load circuitry. Adjusting the potentiometer skews the balance of the load plus or minus a few millivolts of input offset voltage. Datasheets generally recommend a value for the potential, but it is not critical. A much higher resistance potentiometer will cause the change in offset voltage to occur toward the extremes of rotation. Too low a value will reduce the adjustment range. Potentials in the range of +100 percent to 50 percent of the recommended value will likely function satisfactorily.

Notice that the trim circuitry in this example is referenced to the V+ supply. Some op amps have trim circuitry referenced to the V- supply terminal. Connecting the wiper of the potential to the wrong rail or to ground on a dual supply will surely cause problems. Some designers attempt tricky active circuitry to drive these pins. While this is possible, ground-referenced circuitry connected to the trim pins can create power-supply rejection problems.

It is best to use the trim pins only to null the offset of the first amplifier in a signal chain. Generally, that stage has some gain and its offset dominates that of the complete signal chain. If used to correct other large sources of offset in the chain, you could introduce an unwanted temperature drift.

Lacking trim pins, there are other ways to trim offsets in your system. You could inject or sum variable voltages from a potentiometer or other control signal into various points in your signal chain. **Figure 14** shows examples. The trimming voltages shown here should be derived from the power supplies. Regulated supplies are probably sufficient. Unregulated supplies, such as batteries, may not be sufficiently constant or stable.

The improved offset voltage of modern amplifiers often eliminates the need for trimming. Still, there are times when some type of offset adjustment is required. You can be ready with techniques, whether with trim pins or add-on circuitry.

To see this original post with comments, click here.

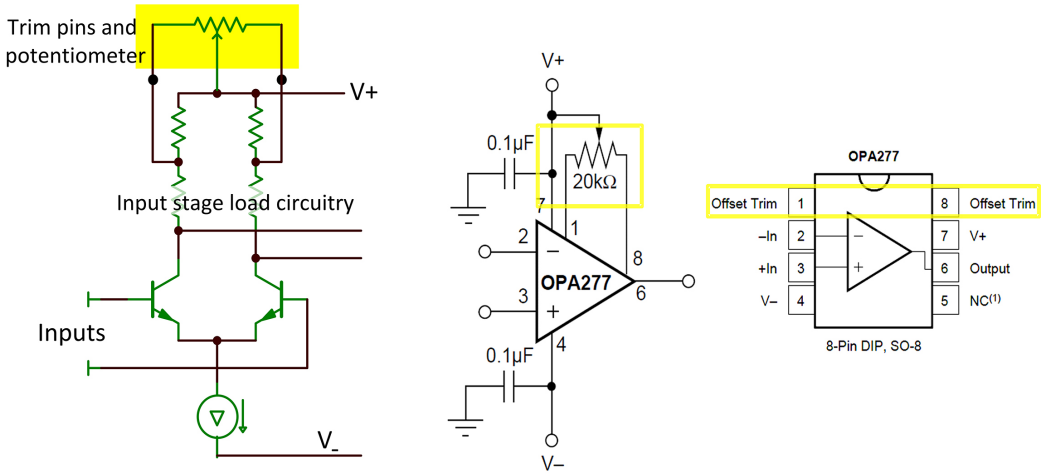

Figure 13: Typical internal circuitry where trim pins connect to the input-stage load circuitry.

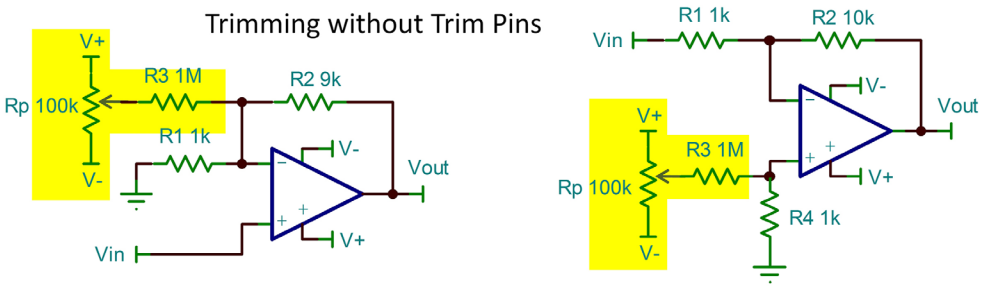

Figure 14: Examples of offset-correction voltages injected into various points of the signal chain.

7. I need high input impedance! Input impedance vs. input bias current

In helping to select operational amplifiers (op amps) and instrumentation amplifiers, I frequently hear, "I need really high input impedance." Oh, really? Are you sure?

It is rare that input impedance (or more specifically input resistance) is an important issue. (Input capacitance, the reactive part of input impedance, is another matter). What is most often needed is low input bias current, I_B. Yes, they are related, but different. Let us sort it out.

A simple model of a single input is a parallel combination of a current source (the input bias current) and an input resistor (**Figure 15**). The resistor causes the input current to vary with input voltage. The input bias current is the input current at a specific input voltage, usually at midsupply.

The input resistance is a measure of the change in input current with a change in input voltage. It is possible to have an ampere of input bias current and still have extremely high input resistance.

TI often provides a typical graph showing input bias current vs. common-mode voltage. A couple of examples are shown in **Figure 16**; you can see that it's not a perfectly straight line. Note that the OPA211 is a bipolar junction transistor (BJT)-input op amp with input bias current cancellation that greatly reduces input bias current – but it is still pretty high. The OPA211's input bias current and high noise current make it an unlikely choice with a source resistance greater than 10 kΩ, so its input resistance of 1.3 GΩ is seldom an issue.

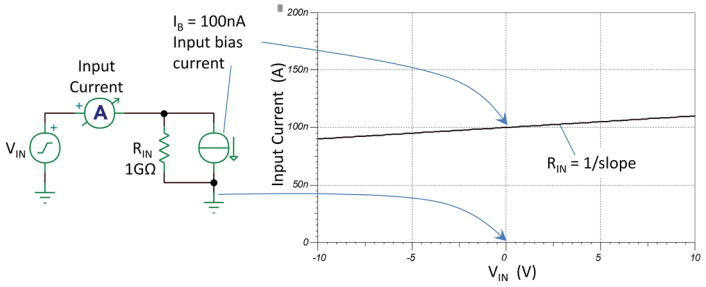

Figure 15: Model of one input terminal is a current source and an input resistor in parallel.

The OPA320 complementary metal-oxide semiconductor (CMOS) op amp has a tiny input bias current, primarily coming from the leakage of its input electrostatic discharge (ESD) protection circuitry. These leakage currents reach a maximum near the rail voltages. CMOS and junction .(JFET)-input amplifiers are generally the best choices when you require a very low input bias current. Yes, the input resistance is high, but it is not generally an important factor in amplifier selection.

There are several ways that input bias current can be detrimental in precision-analog circuitry. Flowing through a source resistance or feedback network resistance, it can contribute $I_B R_S$ to the offset voltage. Flowing in certain sensors and chemical cells such as pH probes, it can polarize the electrodes, creating errors and even causing permanent damage. Input bias current will charge the capacitor of an integrator circuit, creating a ramping output with zero input.

Depending on the sensitivity of your circuit to input bias current, it can be a deciding factor in amplifier selection. Check out typical performance graphs showing variations of I_B with input voltage, with an eye to the particular voltage range of interest. Overtemperature behavior may be particularly important with CMOS and JFET amplifiers, as their I_B generally rises dramatically with increasing temperature.

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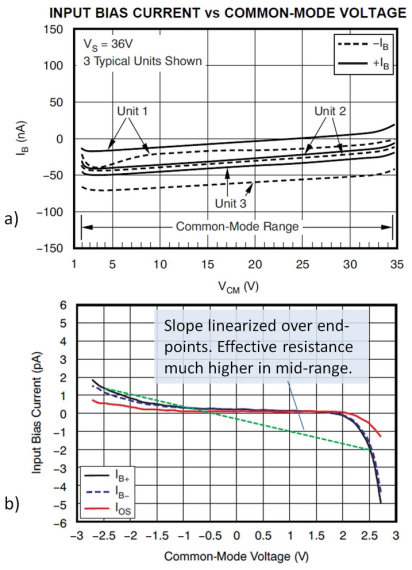

OPA211—low noise bipolar (BJT) op amp with input bias cancellation.

Input resistance = inverse slope:
≈ Δ33V / Δ25nA ≈ 1.3GΩ

OPA320—20MHz CMOS op amp.

Input resistance = inverse slope:
≈ Δ5V / Δ3pA ≈ 1.6e12 Ω

Figure 16: Input bias current vs. common-mode voltage.

8. Input bias current of CMOS and JFET amplifiers

Complementary metal-oxide semiconductor (CMOS) and junction FET (JFET)-input operational amplifiers (op amps) are often selected for their low input bias current (I_B). But there is more to the story than a single line in a specifications table – subtleties that you should be aware of.

The gate of a CMOS transistor (the working input of a CMOS op amp) has extremely low input current. But these fragile gates must be protected from electrostatic discharge (ESD) and electrical overstress (EOS) with additional circuitry that is the primary source of their input bias current. This protection generally includes internal clamp diodes to the supply rails. The OPA320 is an example, shown in **Figure 17a**. These diodes have a small leakage current in the few picoampere range. At an input voltage near midsupply rails, their leakages are pretty well-matched, leaving only a small residual difference current of less than 1 pA that appears as amplifier input bias current.

The relationship of the two diode leakages changes as the input voltage nears the supply rails. Near the bottom rail, for example, D2's reverse voltage nears zero and its leakage drops. D1's leakage will dominate, causing a higher input bias current flowing out of the input terminal. Of course, the opposite occurs as the input approaches the positive supply rail. The input bias current is specified and tested at the midpoint, where leakage is nearly matched and quite low.

The result is an input bias current versus an input voltage that varies, as shown in **Figure 17b**. For any given unit, there is an input voltage where the input bias current is zero (assuming no significant package or circuit layout leakage). In fact, with a rail-to-rail op amp you can often self-bias the input (**Figure 18**); the output will drift to a voltage equal to the zero input-bias-current point. It is an interesting experiment but not a particularly useful circuit.

The story can be different with JFET-input amplifiers such as the OPA140 (**Figure 19**). Here, the gate of the input transistor is a diode junction and its leakage current is often the dominant source of input bias current. The input gate junction is generally larger and therefore leakier than the protection diodes. Thus, the input bias current is more often unidirectional. It can vary and depends on the amplifier.

So, what to conclude? If very low input bias current is important in your circuit, be aware. Look carefully at typical performance graphs to glean all available information. If you operate with input voltages that are near the positive or negative rails, you may have higher input bias current. This leads to another important point – input bias current will increase significantly with temperature.

This discussion applies to most common general-purpose CMOS and JFET amplifiers, but there are special-purpose amplifiers designed for ultra-low input bias current. They use creative protection circuitry with unique pinouts to achieve I_B in the range of 3 fA – three orders of magnitude lower than general-purpose devices.

Examples:

- The LMP7721 3-fA input bias current CMOS op amp.
- The INA116 ultra-low input bias current instrumentation amplifier.

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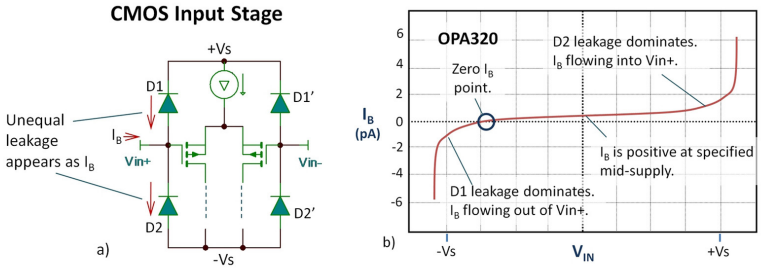

Figure 17: Protecting op amps from ESD and EOS using internal clamp diodes to the supply rail (a); input bias current versus input voltage (b).

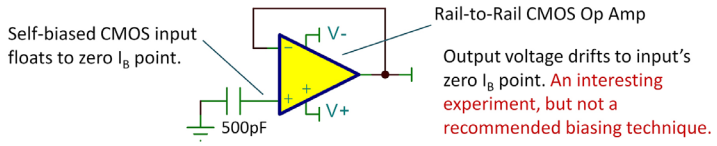

Figure 18: A rail-to-rail CMOS op amp with a self-biased input—not recommended!

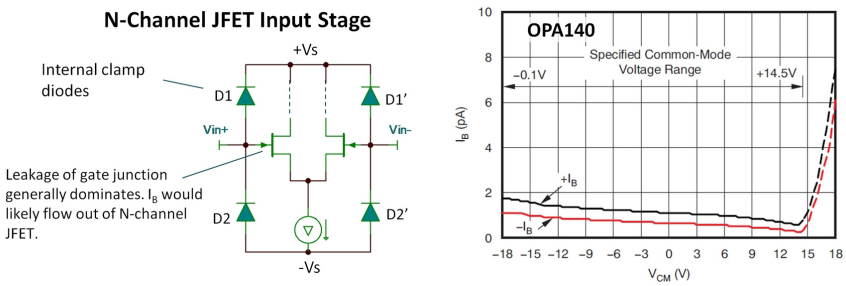

Figure 19: Input bias current is often unidirectional depending on the input amplifier, such as with the JFET-input amplifier shown here.

9. Temperature effects on input bias current

In section 8, I looked at the source of input bias current in complementary metal-oxide semiconductor (CMOS) and junction FET (JFET) amplifiers, finding that it comes from the leakage of one or more reverse-biased P-N junctions. I ended with a caution that these leakages increase significantly with temperature.

The reverse-biased leakage of a P-N junction has a strong positive temperature coefficient, approximately doubling for each 10°C increment in temperature. This exponential increase racks up quickly, as shown in the normalized graph of **Figure 20**. At 125°C, leakage climbs to approximately 1,000 times the room-temperature value.

The rate of increase can vary with diode characteristics, and the doubling of current may occur over a range of 8°C to 11°C. This increased bias current at high temperatures can be a significant problem in some circuits and may be a good reason to select a FET or CMOS operational amplifier (op amp) with a very low room temperature input bias current. In some cases, you may achieve lower I_B at high temperatures with a bipolar-input (BJT) op amp that does not have such a dramatic increase at high temperature.

The leakage generally continues to fall at lower temperatures, but other possible sources of leakage may alter the behavior. These stray leakages may have different temperature dependencies. To be honest, less is known about the behavior below room temperature because the higher leakage at room temperature and above is the greater concern. It is best not to place high confidence in behavior much below room temperature. The important issue at low temperatures is more likely to be possible water condensation, which can cause leakage to rocket upward.

As discussed in section 8, the input bias current of most CMOS op amps comes from the difference in leakage of two input-clamp diodes connected to the power rails. In a perfectly balanced world, the residual difference between two nearly equal leakages still has the same exponential temperature variation; it just starts at a lower initial value. The polarity of I_B is uncertain; and, with small differences in diode behavior, the net current may dip through zero at some temperature (the logarithmic graph shows the absolute value without a sign).

So, what to conclude? If very low input bias current is critical in your FET op amp circuit, carefully consider its increase with temperature. Study all of the specifications and typical performance graphs. Avoid placing sensitive circuitry near heat sources. Make your own measurements, if necessary. For really critical applications, there are special-purpose amplifiers with ultra-low input bias current. They use creative protection circuitry with unique pinouts to achieve I_B in the range of 3 fA at room temperature – three orders of magnitude lower than general-purpose devices.

Examples:

- The LMP7721 3-fA input-bias-current CMOS op amp.
- The INA116 ultra-low-input-bias-current instrumentation amplifier.

To see this original post with comments, click here.

A random quiz: On the film capacitors in **Figure 21**, what is the meaning and purpose of the black bands?

See Page 36 for the answer to this quiz.

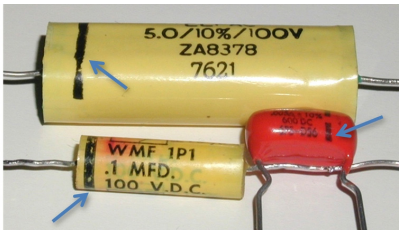

Figure 21: Film capacitors—what is the purpose of the marking stripe?

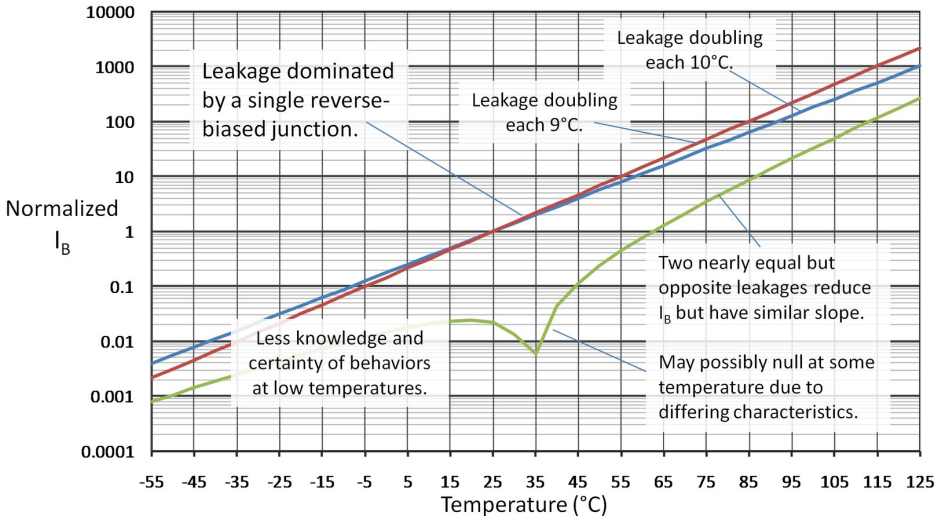

Figure 20: Reverse-biased leakage of a P-N junction approximately doubles with each 10°C increment in temperature.

10. Input bias current cancellation resistors: do you really need them?

Do you add a resistor to match the direct current (DC) resistance at the inputs of your operational amplifier (op amp) circuits? Check the circuits in **Figure 22**. Many of us were instructed to add Rb as "good practice," making its value equal to the parallel combination of R1 and R2. Let us look at the reason for this resistor and consider when it is appropriate and when it is not.

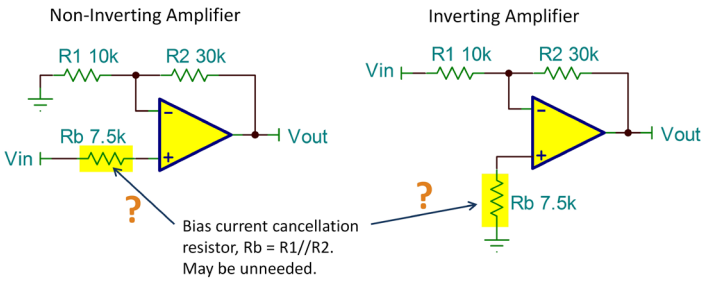

Figure 22: Resistor added to non-inverting input to match the source resistances.

The purpose of Rb is to reduce the voltage offset caused by the input bias current. If both inputs have the same input bias current, equal current flowing through equal resistances will create equal and opposite offset voltages. Thus, input bias current will not contribute to the offset voltage of the circuit. The basic idea has merit in some instances. But before adding Rb, is it always necessary?

Many times, the parallel resistance of R1 and R2 is low enough, and input bias current is low enough, that the offset created without Rb is insignificant. Before adding this resistor, calculate the error. Let us assume for this application that the input bias current of the op amp is 10 nA. Without using Rb, the input-referred offset voltage due to the input bias current will be:

$$\text{Input offset voltage due to } I_B = (10\text{ nA})\,(7.5\text{ k}\Omega) = 75\ \mu\text{V} \qquad (1)$$

Will 75 µV of input offset affect your circuit? Many times the answer will be no, so why add the resistor?

Consider the offset voltage of the op amp you are using. It may be pointless to be concerned with 75 µV if, for example, the offset-voltage specification of your op amp is 1 mV. So compare the error produced by the input bias current to the offset-voltage specification before routinely adding Rb to your circuit.

Transimpedance applications often use high feedback-resistor values to amplify very small currents (**Figure 23**). Here again, you may be tempted to add Rb to balance the resistance at both inputs. But these applications generally use FET- or complementary metal-oxide semiconductor (CMOS)-input op amps. With their very low input bias current, the offset error is generally very small.

Thermal noise produced by Rb and possible external noise pickup at this high-impedance node may be additional reasons to eliminate Rb. With minimal error from the input bias current, why add possible noise to the circuit?

There may occasionally be a clear and valid case for using a bias current cancellation resistor. But many circuits derive no significant benefit, and may even suffer reduced performance.

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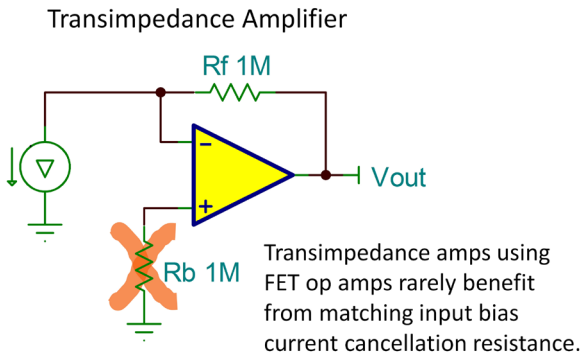
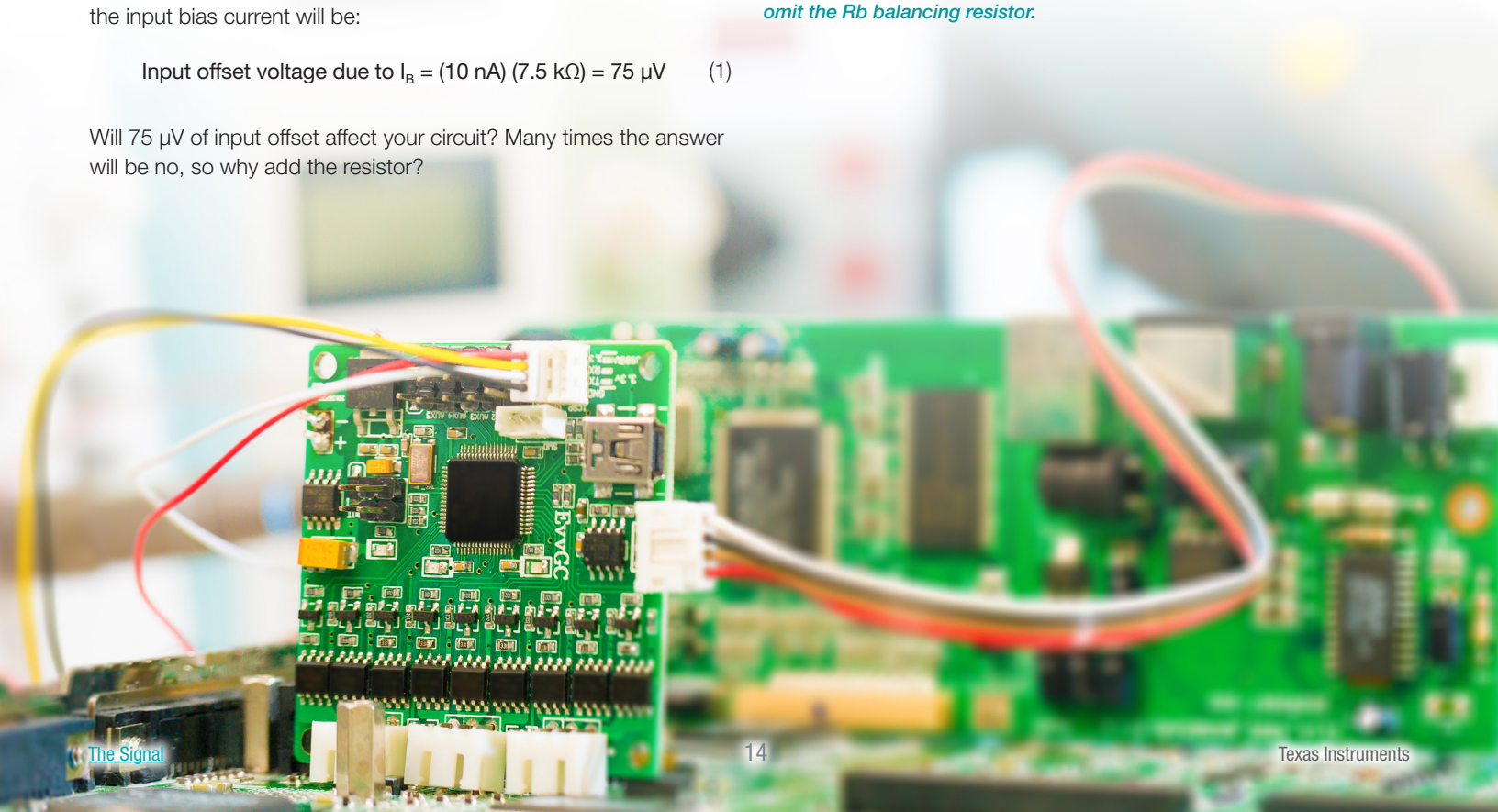


Figure 23: High gain transimpedance circuits using FET op amps should omit the Rb balancing resistor.



11. Internal input bias current cancellation of bipolar op amps

In section 10, I reviewed the use of an input-bias-current cancellation resistor to balance the source resistance at the two inputs of an operational amplifier (op amp). I concluded that this practice is often not necessary and may even be detrimental.

I ended the previous section by saying that there are certain op amps for which this practice is definitely not recommended: amplifiers with bipolar input transistors that have internal input bias current cancellation. Their current sources, I1 and I2, supply base current for the input transistor pair (**Figure 24**). These currents are derived by mirroring carefully matched base currents into the op amp's input terminals.

While these currents are accurately matched to the base current of the input transistor (typically within a few percent), they are not perfect. They leave a small residual input bias current that could be positive or negative. The residual current may be quite different on the two input terminals. They may even be opposite polarities. Any possible benefit from matching source resistance (as in **Figure 25**) relies on nearly matching input bias currents. Internal input bias current cancellation renders this practice useless.

Which op amps have input bias current cancellation? Datasheets sometimes do not make this feature apparent. The effects are generally revealed, however, in the details of input-bias-current specifications.

Figure 26a shows the input-bias-current specification for the OPA209, a low-noise op amp with input-bias-current cancellation. Note that the input bias current is preceded by a ± symbol to indicate that current could flow in either direction, your first hint. Also note that the specifications for input offset current are the same magnitude as the input bias current (actually identical on this op amp). These specifications reveal that this device has internal input bias current cancellation.

Figure 26b shows a hypothetical specification for the OPA209, assuming it did not have bias current cancellation. Note the much larger input bias current. And now, the input offset current is much smaller than the input bias current because the two input bias currents are nearly equal. Depending on the circuit and application, this hypothetical op amp might benefit from the use of a bias current cancellation resistor, as shown in **Figure 24**.

Internal input bias current cancellation is generally found on precision and low-noise op amps with input from bipolar junction transistors (BJTs) – ones that would otherwise have an uncomfortably high input bias current. Internal cancellation makes these amplifiers useful in a wider range of circuits.

Do you ever design circuits that rely on a known polarity of input bias current? It would not be wise with these canceled-input devices, right?

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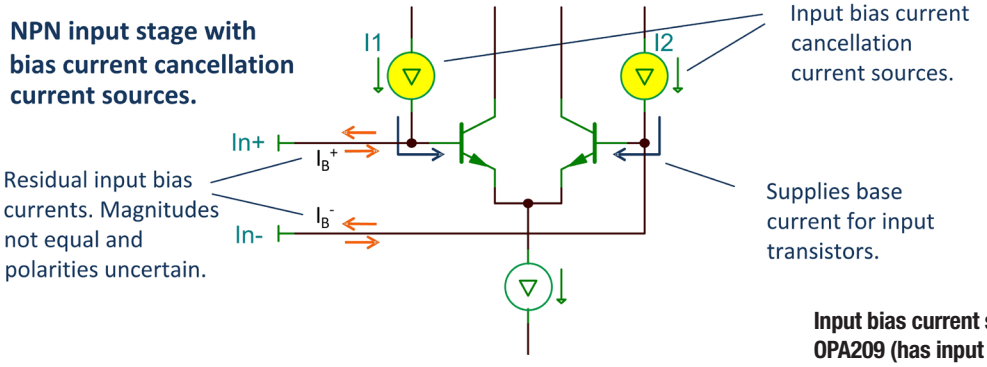

Figure 24: BJTs with internal current sources for input bias current cancellation.

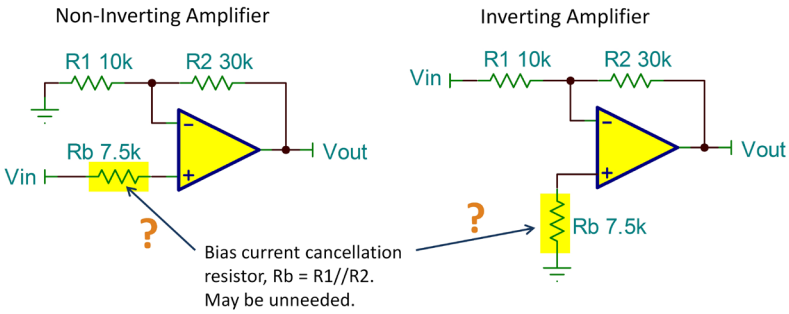

Figure 25: Op amp circuit with bias-current-cancellation resistor added to non-inverting input.

Input bias current specification for OPA209 (has input bias current cancellation).

Input Bias Current	Min	Typ	Max	Unit
Input bias current		±1	±4.5	nA
Input offset current		±0.7	±4.5	nA

± Indicates bias current could flow in either direction.

Input offset current same or similar to input bias current.

(a)

Hypothetical specification for same op amp assuming no bias compensation.

Input Bias Current	Min	Typ	Max	Unit
Input bias current		40	80	nA
Input offset current		1.5	5	nA

Offset current, $I_{OS} = (I_B^+) - (I_B^-)$

Input offset current much smaller than input bias current.

(b)

Figure 26: Specifications of an op amp with input-bias-current cancellation (a); and a similar op amp without input-bias-current cancellation (b).

12. Why op amps oscillate: an intuitive look at two frequent causes

Bode plots are great analytical tools, but you may not find them intuitive. This is a purely qualitative look at frequently encountered causes for operational amplifier (op amp) instability and oscillations.

The perfectly damped response in **Figure 27** occurs with no delay in the feedback signal reaching the inverting input. The op amp responds by ramping toward the final value, gently slowing down as the feedback signal detects closure on the proper output voltage.

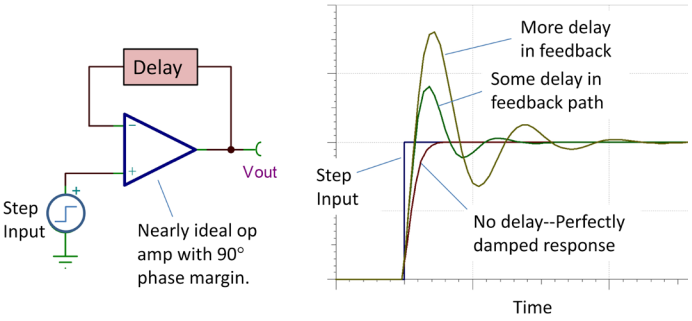

Figure 27: Op amp step response with varying delay inserted in the feedback path.

Problems develop when the feedback signal is delayed. With delay in the loop, the amplifier does not immediately detect its progress toward the final value. It overreacts by racing too quickly toward the proper output voltage. Note the faster initial ramp rate with delayed feedback. The inverting input fails to receive timely feedback that it indeed reached and passed the proper output voltage. It overshoots its mark and requires several successively smaller polarity corrections before finally settling.

A little delay and you merely get some overshoot and ringing. Too much delay and these polarity corrections continue indefinitely – an oscillation.

The source of delay is often a simple low-pass resistor-capacitor (RC) network. OK, it is not a constant delay for all frequencies, but the gradual phase shift of this network from 0° to 90 degrees produces a first-order approximation of time delay, t_d = RC.

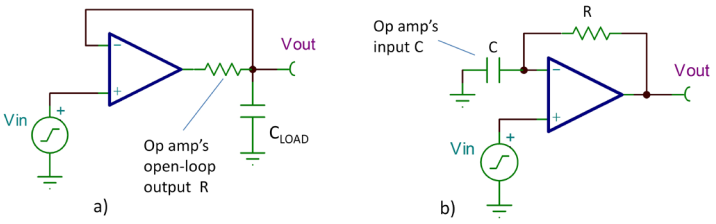

Figure 28: Phase shift (delayed feedback) commonly occurs in two ways: Due to capacitive load (a); or with capacitance at the inverting input terminal (b).

There are two commonly encountered situations where this RC network unintentionally sneaks into circuits. The first is with a capacitive load (**Figure 28a**). The resistor is the op amp's open-loop output resistance. The capacitor is, of course, the load capacitance.

In the second case (**Figure 28b**), the feedback resistance and the op amp's input capacitance form the RC network. Circuit-board connections also contribute to the capacitance at this sensitive circuit node. Note that the two circuits have identical feedback loops. The only difference is the node at which the output is taken. From a loop-stability standpoint, they can create the same issues. And these two causes of delayed feedback often occur in combination – a bit of both can be double trouble.

The second case needs a bit more comment: A feedback resistor is not necessary for the simple G = 1 buffer, so the more common situation is a gain configuration using a feedback resistor and resistor to ground (**Figure 29**). The parallel combination of these resistors forms the effective R in the RC circuit.

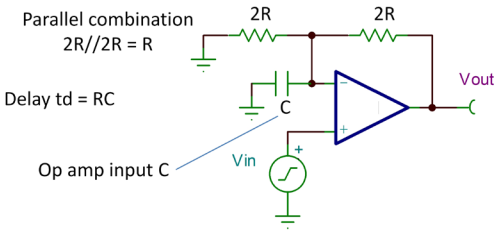

Figure 29: The parallel resistance of the feedback network form the R in an RC circuit.

There is more to learn with Bode analysis of feedback amplifiers. Still, this simple, intuitive view of how delay or phase shift in the feedback path affects stability can help you diagnose and solve the most common stability problems.

To see this original post with comments, click here.

13. Taming the oscillating op amp

In section 12, I looked at two very common reasons for oscillations or instability in operational amplifier (op amp) circuits. The ultimate cause of both was delay or phase shift in the feedback path.

A simple noninverting amplifier can be unstable or have excessive overshoot and ringing if the phase shift or delay created by the op amp's input capacitance (plus some stray capacitance) reacting with the feedback network resistance is too great (**Figure 30**). You may be able to make some improvements by reducing stray capacitance at this node, minimizing the circuit-board trace area of this connection. For a given op amp, input capacitance (differential plus common-mode capacitance) is a fixed value – you are stuck with it. You can, however, reduce the resistances of the feedback network proportionally to keep the gain identical.

Reducing the resistances moves the pole created by this capacitance to a higher frequency and decreases the delay time constant. Reducing the resistances to 5 kΩ and 10 kΩ in this example is a big improvement but still produces approximately 10-percent overshoot with ringing. It also creates additional load on the op amp, so you cannot take this solution too far. The sum of the two resistors is a load on the op amp, and you would not want it to be too low.

The better solution is likely to be a capacitor, Cc, connected in parallel with R2 (**Figure 31**). When R1×Cx = R2×Cc, the voltage divider is compensated and the impedance ratio is constant for all frequencies. There will be no phase shift or delay in the feedback network.

You can liken the feedback network to the compensated attenuator in a 10-times oscilloscope probe (**Figure 32**). It is the same concept. A variable capacitor in the probe allows adjustment to make the two time constants equal. Note that the response of this scope probe does not ever appear unstable, even when improperly adjusted. Why? Because it is not inside a feedback loop.

Just as you can adjust one of the capacitors in a scope probe to fine-tune the compensation, you may also need to adjust the value of Cc shown in **Figure 31**. You may not precisely know the capacitance, Cx, due to the uncertain effects of stray capacitance. Furthermore, you may want to tune the response of the circuit to meet your requirements, with a little bit of overshoot for improved speed and bandwidth.

Another common cause of instability is an op amp with capacitive load. Again, this situation produces phase shift in the loop (delayed feedback) that is the root of the problem. This one is tricky because open-loop output resistance is internal to the op amp. You cannot connect a compensating capacitor across this resistor. In fact, it is not really a resistor at all; it is an equivalent output resistance of the op amp circuitry.

Consider your last oscillating op amp. Can you explain the problem with delayed feedback?

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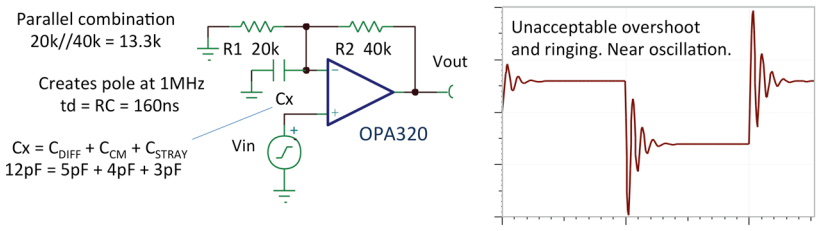

Figure 30: Excessive output overshoot and ringing indicates possible instability.

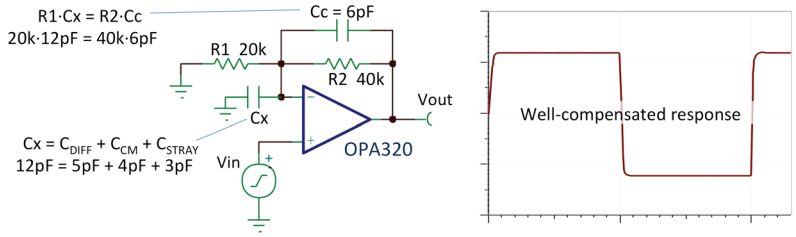

Figure 31: A capacitor, Cc, connected in parallel with R2 avoids phase shift in the feedback signal path.

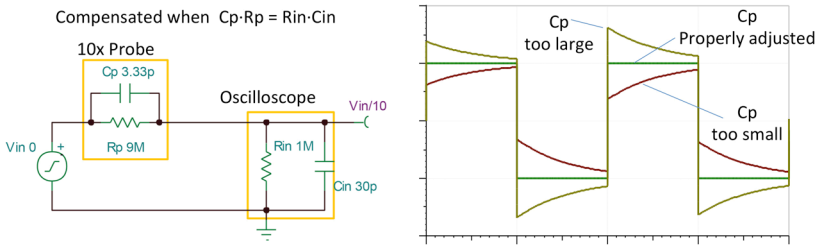

Figure 32: A feedback network is much like a compensated attenuator in a 10x oscilloscope probe.

14. Taming oscillations: the capacitive load problem

I have been looking at the stability of operational amplifiers (op amps), considering how phase shift (or call it delay) in the feedback path can cause problems. Picking up from section 12 and section 13, stability with a capacitive load is a tricky case.

The troublemaker, the open-loop output resistance (Ro) of the op amp, is not actually a resistor inside the op amp. It is an equivalent resistance dependent on the internal circuitry of the op amp. There is no chance to change it without changing the op amp. C_L is the load capacitance. If you want to drive a certain C_L, you are stuck with the pole created by Ro and C_L. A 1.8-MHz pole inside the feedback loop of a 20-MHz op amp in G = 1 spells trouble. Check it out in **Figure 33**.

Solutions to this issue have a common theme – they slow the amplifier down. Think about it: The loop has a fixed amount of delay, from Ro and C_L. To accommodate this delay, the amplifier must respond more slowly so that it does not speed past, overshooting a desired final value.

A good way to slow things down is to put the op amp in a higher gain. Higher gain decreases the bandwidth of the closed-loop amplifier. **Figure 34** shows the OPA320 driving the same 1-nF load but in a gain of 10. The response to a small step dramatically improves but is still marginal. Increase the gain to 25 or more, and it would look pretty good.

But here is another trick. **Figure 35** is still a gain of 10 but with Cc added, slowing things down a bit more in just the right way. Not enough Cc and the response looks more like **Figure 34.** Too much Cc and you are headed for trouble, more like **Figure 33**.

Getting this compensation just right is solving a "rate-of-closure" issue – Bode analysis. A bit of intuition is helpful with these problems, but if you want to advance to the next level of phase-compensation competence, you need Mr. Bode.

My colleagues, Pete Semig and Collin Wells, did a great job distilling the subject of op amp stability and Bode analysis to its essence.

To see this original post with comments, click here.

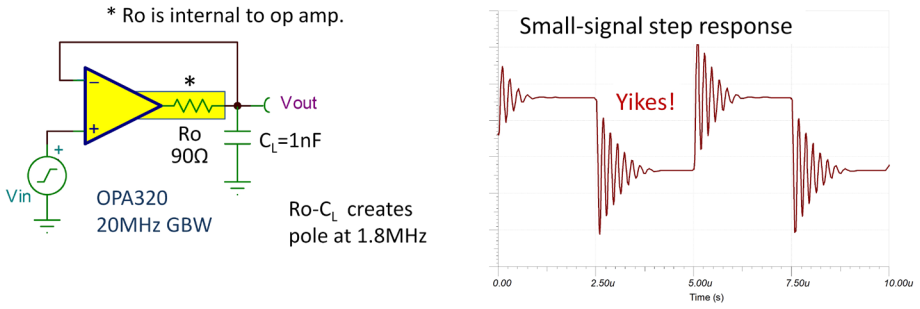

Figure 33: A 1.8-MHz pole inside the feedback loop of a 20-MHz op amp in G = 1 (left) can result in an undesirable small-signal step response (right).

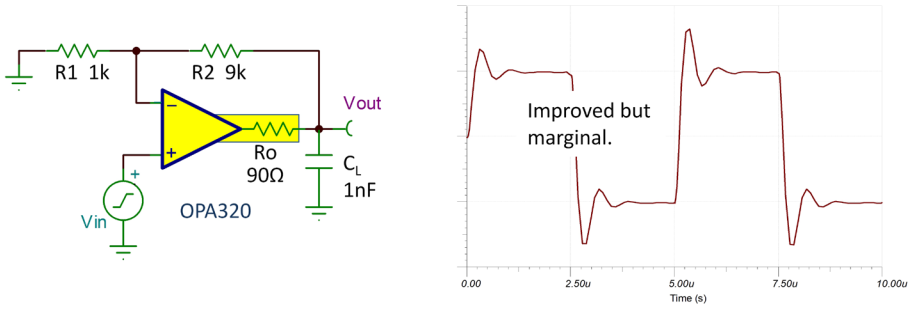

Figure 34: Using an op amp in a higher gain of 10 decreases the bandwidth of the closed-loop amplifier; however, the improvement is marginal.

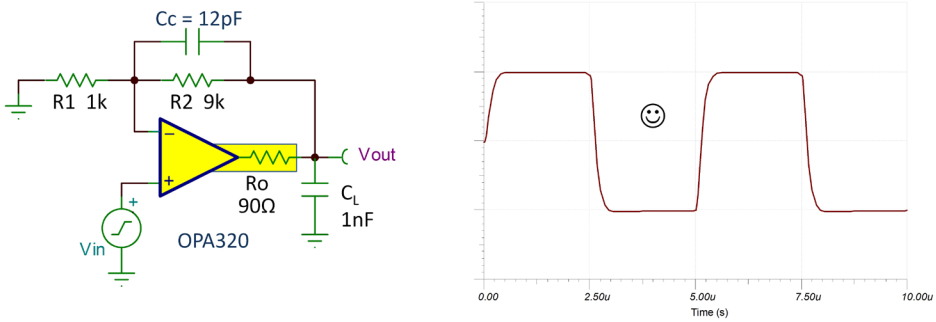

Figure 35: Using the same configuration, adding a Cc of 12 pF in parallel with the feedback resistor produces an ideal response.

15. SPICEing op amp stability

The simulation program with integrated circuit emphasis (SPICE) is a useful tool to help check for potential circuit-stability problems. Here is one simple way to do it.

Figure 36 shows a noninverting amplifier using the OPA211 with a couple of minor variations common in many applications. R3-C1 is an input filter. R4 is an output resistor to protect against abuse when connected to the outside world. C_L models a five-foot cable.

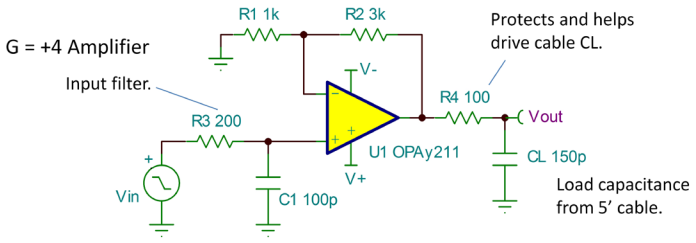

Figure 36: A noninverting amplifier with minor variations common to many applications.

Checking the response to a small-signal step function or square wave is the quickest and easiest way to look for possible stability problems. **Figure 37** shows the simulation circuit. Notice that the input terminal is connected to ground and the input test signal is connected directly to the noninverting input. The input filter would slow the input edge of a step function. If you want to know how a bell rings, hit it with a hammer, not a rubber mallet.

The response is probed at the output of the operational amplifier (op amp), not just the V_{OUT} node of the circuit. R4 and C_L filter the output response so that V_{OUT} will not show the true overshoot of the op amp. To check stability, you want to know what the op amp is doing.

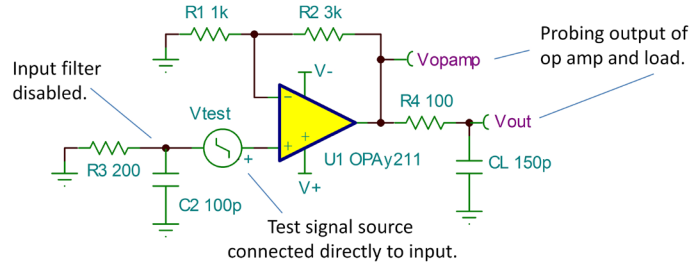

Figure 37: A simulation circuit with the input terminal connected to ground and the input test signal connected directly to the noninverting input.

Notice that the amplitude of the applied step is 1 mV (creating a 4-mV step at the output). You want the small-signal step response. A large input step that induces slewing will have less overshoot and will not clearly reveal potential instability.

The simulation shows approximately 27-percent overshoot at the op amp's output – too much for you to be comfortable that this circuit will be stable under all conditions (**Figure 38**).

Assuming a second-order stability system, this overshoot would indicate a phase margin of approximately 38 degrees. Also notice that the frequency response shows considerable amplitude peaking, another sign of potential instability. The peaking occurs at 14 MHz – the inverse of the period of the ringing in the time domain. A commonly accepted guideline for reasonable stability is a phase margin of 45 degrees (or greater), which translates to 20-percent (or less) overshoot (**Figure 39**).

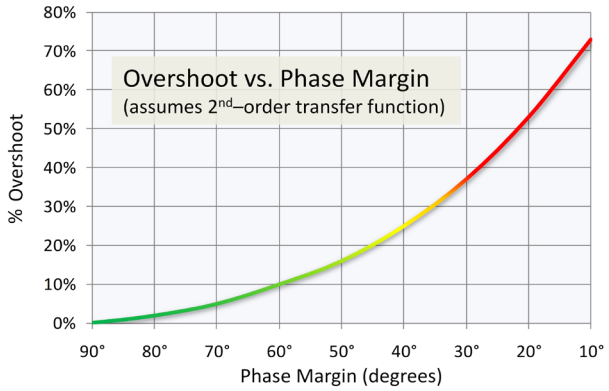

Figure 39: A 20-percent overshoot indicates approximately 45° phase margin—often considered to be satisfactory for most circuits.

There are fancier analyses that you can do with SPICE – Bode analysis by breaking the loop, finding phase and gain margins. But for most relatively simple circuits (a feedback loop involving one op amp), this approach is a very good indicator of possible problems.

Of course, any SPICE simulation relies on the accuracy of the op amp's macromodel. Our best SPICE models are excellent but not perfect. Furthermore, circuit variation, nonideal components, circuit-board layout parasitics, poor supply bypassing – all can affect the circuit. That's why you build it, test it, compare with simulations and optimize. SPICE is a useful tool, valuable but not perfect.

The late Bob Pease, a true analog guru, wrote skeptically about the use of SPICE. Check out this blog on his opinions: SPICE It Up! … but does Bob Pease say no? To see this original post with comments, click here.

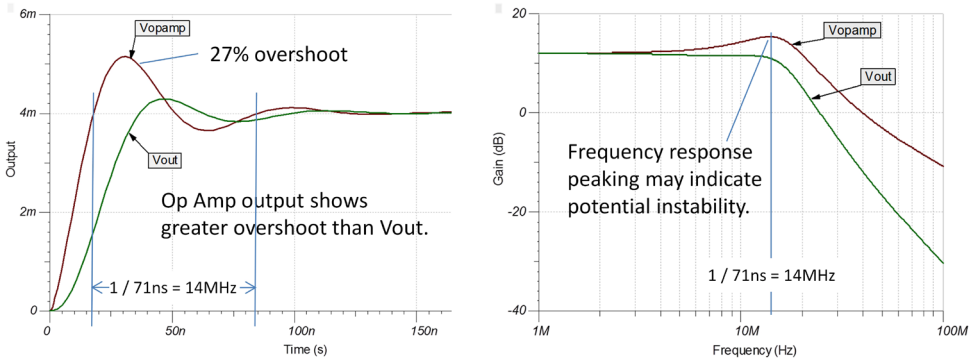

Figure 38: An op amp circuit with 27-percent overshoot may be marginally unstable.

16. Input capacitance: Common mode? Differential? Huh?

The input-capacitance specifications of operational amplifiers (op amps) are often confused or ignored. Let us clarify how to best use these specifications.

The input capacitance at the inverting input can affect the stability of an op amp circuit by causing phase shift – a delay of the feedback reaching the inverting input. The feedback network reacts with the input capacitance to create an unwanted pole. Scaling the impedance of the feedback network in relation to the input capacitance is an important step to assure a stable amplifier circuit. But which capacitance matters – differential? Common mode? Both?

The input capacitance of an op amp is generally found in an input-impedance specification showing both differential and common-mode capacitance (**Table 4**).

OPA1652

Input Impedance	Min	Typ	Max	Units
Differential	—	100 // 6	—	MΩ // pF
Common-Mode	—	6000 // 2	—	GΩ // pF

Table 4: Input-impedance specification showing both differential and common-mode capacitance.

Input capacitance is modeled as common-mode capacitance from each input to ground and differential capacitance between the inputs; see **Figure 40**. Though there is no ground connection on an op amp with dual supply voltages, consider the common-mode capacitances as being connected to the V– supply terminal, the alternating current (AC) equivalent of ground.

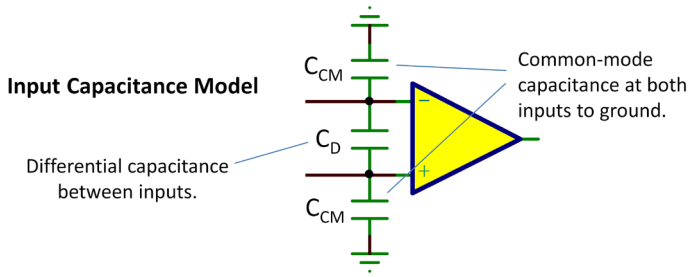

Figure 40: Input capacitance modeled as common-mode capacitance from each input to ground and differential capacitance between the inputs.

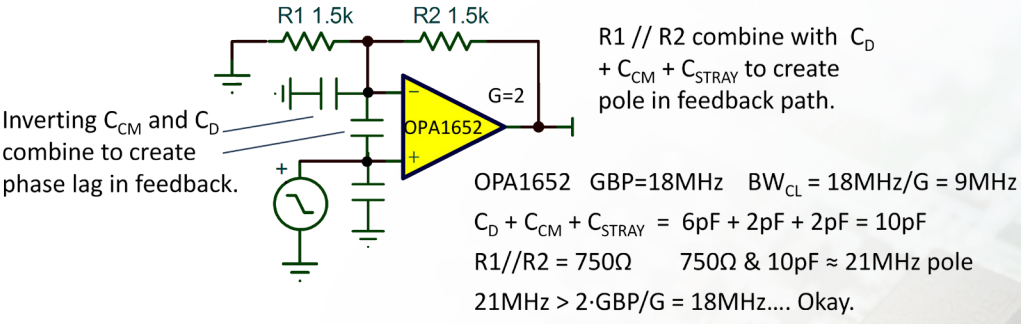

Figure 41: Calculation of pole due to input capacitance and feedback network.

At high frequencies where stability is a concern, the op amp has little open-loop gain, and substantial AC voltage exists between the two inputs. This causes the differential capacitance to combine with the inverting common-mode capacitance to alter the phase of the feedback signal. So add the two capacitances that connect to the inverting input. Include an estimate of stray wiring capacitance (perhaps around 2 pF). This total capacitance reacts with the parallel impedance of the feedback network (R1//R2) to create a pole (**Figure 41**).

A guideline: The frequency of this pole should be greater than two times the closed-loop bandwidth of the amplifier. A pole at two times the closed-loop bandwidth will reduce the phase margin of the circuit by approximately 27°. This is generally OK for most circuits in a closed-loop gain of two or greater. Applications with critical settling requirements or capacitive loads may require even greater margin. Reduce the feedback network impedance or consider adding a capacitor across the feedback capacitor, R2.

Today's general-purpose op amps often have wider bandwidths, from 5 MHz to 20 MHz and more. Feedback network resistances that may have been OK with 1-MHz op amps can now create problems – a reason to be diligent when checking the stability of your designs.

SPICE simulation is very helpful in checking sensitivities to input capacitance and feedback impedance, and good op amp macromodels accurately model input capacitances. A transient response check with a 1-mV input step should not cause excessive overshoot and ringing. But remember: Reality always trumps guidelines and simulations. This type of circuitry may require fine-tuning in a final circuit layout.

To see this original post with comments, click here.

17. Op amps ... G = 1 stable and decompensated

Unity-gain-stable operational amplifiers (op amps) are stable in the common G = +1 configuration, returning 100 percent of the output signal back to the inverting input. While it would be incorrect to call this truly a "worst case" for stability, you could reasonably call it a very common, testy case.

Decompensated op amps have smaller compensation capacitors that yield wider gain bandwidth (GBW) and faster slew rates. While higher speed normally demands more power, the same basic op amp can be significantly faster while operating on the same current. But they are not unity gain stable – they must be used in noise gains significantly greater than unity.

Figure 42 shows the critical portion of a gain vs. frequency graph for an idealized pair of unity-gain-stable and decompensated op amps. The decompensated version has five times the GBW – 10 MHz vs. 2 MHz. Slew rate gets the same boost. Note that the unity-gain bandwidth of the unity gain stable op amp is slightly less than its GBW, a common behavior. The unity-gain bandwidth of the decompensated amplifier is half its GBW. You have no business operating this amplifier with noise gain near the unity-gain bandwidth because a second pole at 3 MHz greatly affects the gain/phase behavior in this region. Phase margin would be poor or nonexistent.

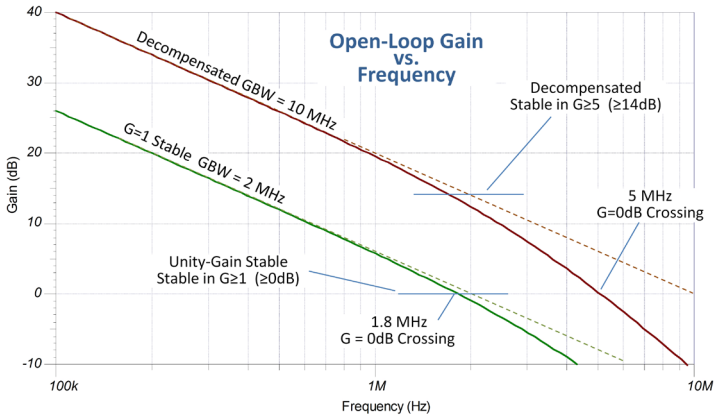

Figure 42: Graph of open-loop gain versus frequency for an idealized pair of unity-gain stable and decompensated op amps.

Decompensated op amps seem to hold a certain mystery, leaving some users uncertain about whether their circuits will be stable. **Figure 43a** shows a common misstep. Although this amplifier is connected in a signal gain of -10, a feedback capacitor rolls off the response at high frequency. This capacitor can be a virtual short circuit at high frequency where stability issues are a concern – unity gain. It is OK to use a small feedback capacitor to compensate the feedback network for flat gain, but a larger cap that rolls off response is sure to create problems.

Likewise, the multiple-feedback filter in **Figure 43b** invites trouble regardless of the low-frequency gain of the filter. The integrator (**Figure 43c**) is yet another application not suited to decompensated op amps.

TI has improved its op amp designs. We are smarter now and we have much better integrated circuit (IC) processes. With a few hundred microamperes, we can now make an amplifier that once required a couple of milliamperes. So sometimes a modern unity-gain-stable op amp may come very close to, or even beat, the speed/power of an older decompensated amp. Still, a decompensated op amp may be the best solution for a demanding application.

Let me be clear, I am not trying to urge you to select decompensated op amps over unity-gain-stable op amps. Each has merits, and you get to "vote" with your design choices. Whatever your selection, you should clearly understand the differences and issues. If you are unsure, help is available in the Precision Amplifiers forum on TI's E2E Community.

Here are some examples of decompensated and unity-gain-stable op amp pairs:

- OPA228 (OPA227 unity-gain-stable version) precision, low-noise, bipolar junction transistor (BJT) op amp.
- OPA637 (OPA627 unity-gain-stable version) precision, high-speed, junction FET (JFET) op amp.
- OPA345 (OPA344 unity-gain-stable version) rail-to-rail, CMOS op amp.
- LMP7717 (LMP7715 unity-gain-stable version) 88-MHz, CMOS op amp.

To see this original post with comments, click here.

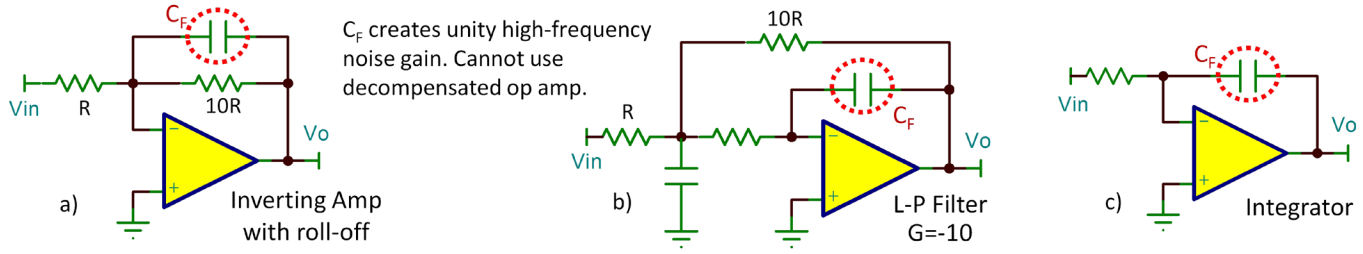

Figure 43: Using a decompensated op amp with a feedback capacitor to roll off the response at high frequency can lead instability (a); a multiple-feedback filter encounters problems irrespective of the filter's frequency gain (b); and an integrator is also unsuitable for decompensated op amps (c).

18. The inverting attenuator G = –0.1: is it unstable?

Unity-gain-stable operational amplifiers (op amps) are stable in a gain of one or greater, but not less, right? What to do (**Figure 44**)?

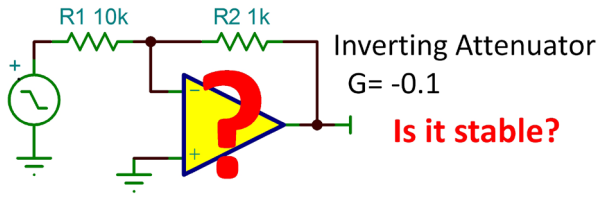

Figure 44: Example of an inverting attenuator.

OK, here is the short answer: an inverting attenuator is stable! You want to know why, right? There are a couple of ways to look at this issue, and a quick look may add clarity to general stability issues.

Consider this: If G = –0.1 were unstable, then even lower gain should be worse, right? Let us draw a circuit: a unity-gain amplifier with a 1-Ω feedback resistor, shown in **Figure 45**. Then consider possible circuit-board leakage forming an input resistor, R1 = 10 GΩ. This is a stray "input signal" amplified at very low inverting gain. Is it unstable? Certainly not! It is just a unity gain buffer with virtually no input. Stable.

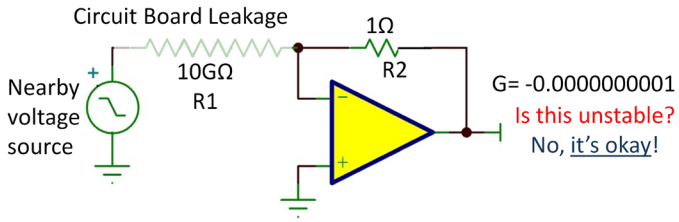

Figure 45: A unity-gain amplifier circuit with a 1-Ω feedback resistor is stable.

Think of the stability of an op amp as related to how much output signal is fed back to the inverting input. Stability experts refer to this feedback factor as beta (β). In unity gain, 100 percent of the output voltage is returned to the inverting input, so β is one. The example in **Figure 45** is essentially the same with nearly all of the output signal fed back to the inverting input.

Figure 46a shows an inverting amplifier and **Figure 46b** shows a noninverting amplifier. The circuits are the same; the input signal is just applied to different nodes. Both circuits return the same amount of output signal to the inverting input so their stability behavior is the same. β is the same.

Op amp wonks also use the term "noise gain" – so named because the op amp's voltage noise is amplified to the output by this factor. It is just another way to quantify the amount of feedback. An op amp circuit prone to oscillations or instability is incited by its own internal noise, amplified and fed back to the inverting input. The inverting amplifier, **Figure 46a**, has the same noise gain, β, and therefore the same stability behavior as its noninverting cousin, even though the input signal gain is different.

Are there circuits with noise gains less than one? Is β ever greater than one? Noise gains less than unity and β greater than one occur when gain is included in the feedback loop. Multiple amplifiers in a larger feedback loop, such as a control system, can face this issue. It also occurs when a transistor (common-emitter or common-source configuration) is included inside the feedback loop of an op amp. These circuits can have tricky stability problems.

Of course, there are other possible causes of oscillations or instability in an inverting attenuator. Capacitive load, excessively high resistor values or too much capacitance at the inverting input can cause instability – but these are unrelated to the basic inverting-attenuator configuration. Misconceptions about the "dangers" of the inverting attenuator persist. Relax. Simulate stability in TINA-TI software or your favorite SPICE program to confirm it. And if you have doubts or problems, check with the experts in the Precision Amplifiers forum on TI's E2E Community.

To see this original post with comments, click here.

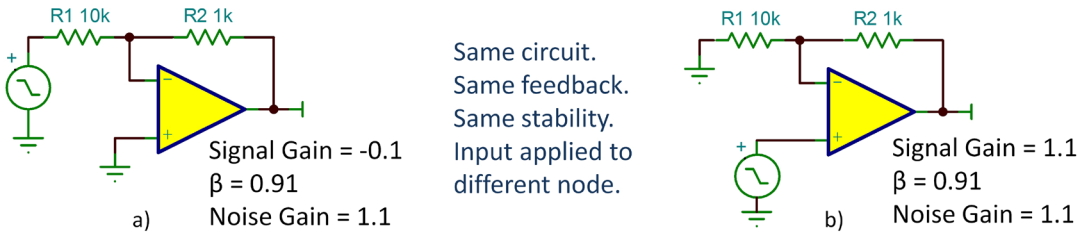

Figure 46: These two circuits, an inverting amplifier (a) and noninverting amplifier (b) have the same feedback factor and stability issues, but with the input signal are applied to different nodes.

19. Simulating gain bandwidth: the generic op amp model

It may not always be obvious how the gain-bandwidth product (GBW) of an operational amplifier (op amp) may affect your circuits. Macromodels have a fixed GBW. Though you can look inside these models, it is best not to tinker with them. What to do?

You can use a generic op amp model in the simulation program with integrated circuit emphasis (SPICE) to check your circuits for sensitivity to GBW. Most SPICE-based circuit simulators have a simple op amp model that you can easily modify. **Figure 47** shows one in TINA-TI software.

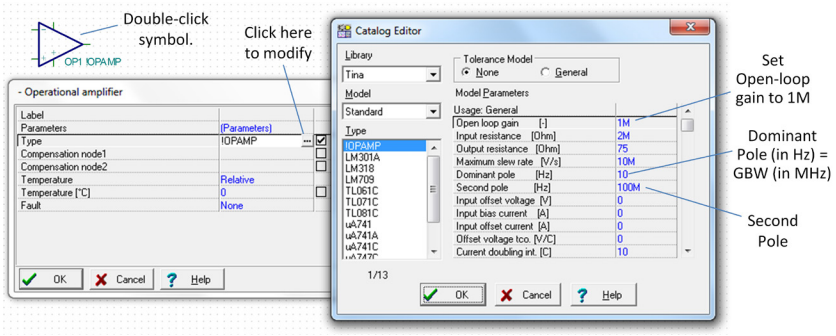

Figure 47: Using TINA-TI software to create a generic op amp model in SPICE to check circuits for sensitivity to GBW.

First, set its direct current (DC) open-loop gain to 1 M (120 dB). Then, a dominant pole frequency (entered in hertz) will create a GBW of the amplifier in megahertz. In this example, a 10-Hz dominant pole creates a GBW of 10 MHz. **Figure 48** shows the open-loop response for three different GBWs: 5 MHz, 10 MHz and 100 MHz.

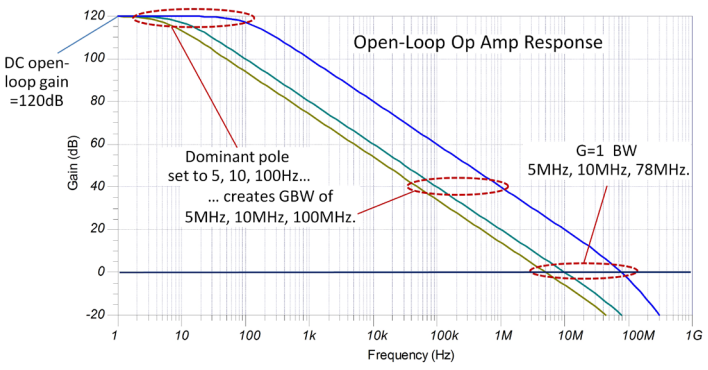

Figure 48: Open-loop response with GBWs of 5 MHz, 10 MHz and 100 MHz.

Note that that this simple model also includes a second pole (some folks call it a nuisance pole). In some cases, you may want to make this second pole a very high frequency, such as 10 GHz. This will create an ideal 90 degrees phase margin for any reasonable GBW. In this example, I set the second pole at 100 MHz, equal to the highest GBW that I am simulating. You can see the effect of this second pole in the 100-MHz GBW response, causing the open-loop response to bend downward at 100 MHz. It causes the unity-gain bandwidth to pull in to approximately 78 MHz, similar to what you might see with a real op amp of this GBW. Unity-gain bandwidth and GBW of a real op amp are not necessarily the same number.

Active filter designs can be tricky to judge GBW requirements and are a good case for using this technique. WEBENCH® Filter Designer, used to design the Chebyshev filter in **Figure 49**, provides GBW recommendations, but its guidelines may be more stringent than needed in some circumstances. For this design, it recommends a 100-MHz or greater GBW to achieve nearly ideal filter-design characteristics. I simulated the design using the three GBWs shown in **Figure 48**: 5 MHz, 10 MHz and 100 MHz. With these results, you might decide that a GBW less than 100 MHz could be satisfactory. For final simulations, you should use the macromodel for the op amp you select.

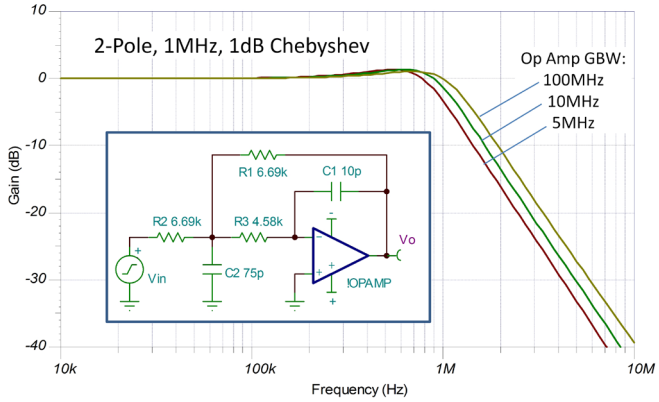

Figure 49: A Chebyshev filter designed in WEBENCH Filter Designer software, but GBW may be more stringent than necessary.

I used the parameter-stepping function in TINA-TI software, varying the dominant pole to change the GBW. Other simulators have similar capability. Of course, you could change parameters manually, too. Either way, varying the GBW of a generic op amp model will give you some insight on its effect in your circuits.

To see this original post with comments, click here.

20. Slew rate: the op amp speed limit

Slewing behavior of operational amplifiers (op amps) is often misunderstood. It is a meaty topic, so let us sort it out.

The input circuitry of an op amp circuit generally has a very small voltage between the inputs – ideally zero, right? But a sudden change in the input signal temporarily drives the feedback loop out of balance, creating a differential error voltage between the op amp inputs. This causes the output to race off to correct the error. The larger the error, the faster it goes; that is, until the differential input voltage is large enough to drive the op amp into slewing.

If the input step is large enough, the accelerator is jammed to the floor. More input will not make the output move faster. (**Figure 50** shows why in a simple op amp circuit.) With a constant input voltage to the closed-loop circuit, there is zero voltage between the op amp inputs. The input stage is balanced, and the current IS1 splits equally between the two input transistors. With a step-function change in V_{IN} greater than 350 mV for this circuit, all of the IS1 current is steered to one side of the input transistor pair. That current charges (or discharges) the Miller compensation capacitor, C1. The output slew rate (SR) is the rate at which IS1 charges C1, equal to IS1/C1.

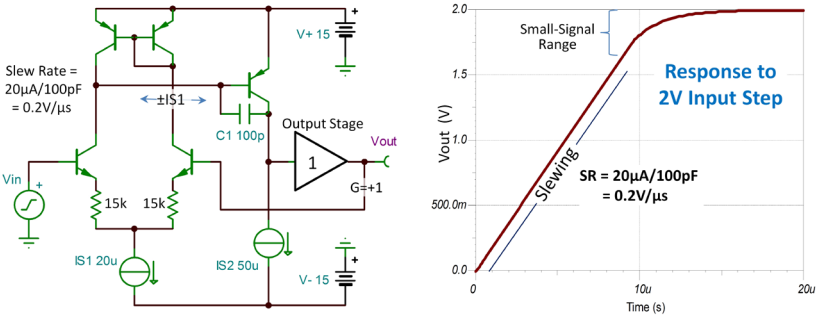

Figure 50: A large change in the input signal creates an output slewing condition.

There are variations, of course. Op amps with slew enhancement add circuitry to detect this overdriven condition and enlist additional current sources to charge C1 faster – but they still have a limited slew rate. The positive and negative slew rates may not perfectly match. They are close to equal in this simple circuit, but this can vary with different op amps. The voltage needed to slew an input stage (350 mV for this design) varies from approximately 100 mV to 1 V or more, depending on the op amp.

While the output is slewing, it cannot respond to incremental changes in the input. The input stage is overdriven and the output rate-of-change maxes out. But once the output voltage nears its final value, the error voltage across the op amp inputs reenters the linear range. Then the rate of change gradually reduces to make a smooth landing at the final value.

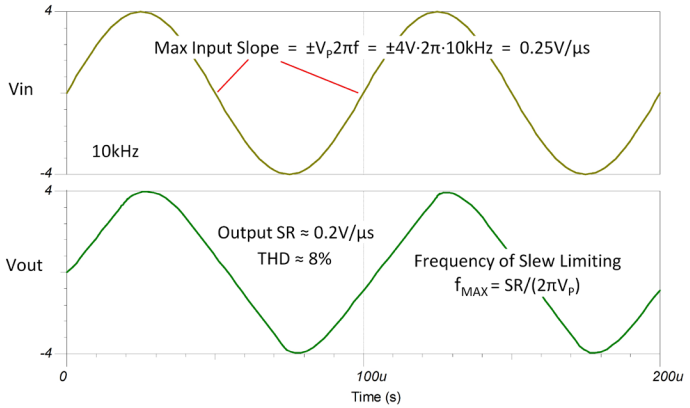

Figure 51: A sine wave shown accurately reproduced (top) and at the onset of slewing (bottom).

There is nothing inherently wrong with slewing an op amp – no damage or fines for speeding. But to avoid gross distortion of sine waves, you should limit the signal frequency and/or output amplitude so that the maximum slope does not exceed the amplifier's slew rate. **Figure 51** shows that the maximum slope of a sine wave is proportional to VP and frequency. With 20 percent less than the required slew rate, the output is distorted into a nearly triangle shape.

Large-signal square waves with very fast edges tilt on the rising and falling edges according to the slew rate of the amplifier. The final portion of a rising or falling edge will have rounding as the amplifier reaches its small-signal range, as shown in **Figure 50**.

In a noninverting circuit, a minimum 350-mV step is required to make this op amp slew, regardless of gain. **Figure 51** shows the slewing behavior for a 1-V input step with gains of 1, 2 and 4. The slew rate is the same for each gain (**Figure 52**). In G = 1, the output waveform transitions to small-signal behavior in the final 350 mV. In G = 2 and G = 4, the small-signal portion is proportionally larger because the error signal fed back to the inverting input is attenuated by the feedback network. If connected in a gain greater than 50, this amplifier would be unlikely to slew because a 350-mV step would overdrive the output.

Slew rate is usually specified in voltage per microseconds, perhaps because early general-purpose op amps had slew rates in the range of 1 V/µs. Very high-speed amplifiers are in the 1,000-V/µs range, but you would rarely see it written as 1 kV/µs or 1 V/ns. Likewise, a nanopower op amp might be specified as 0.02 V/µs but seldom as 20 V/ms or 20 mV/µs. There's just no good reason why for some things; it is just the way we do it.

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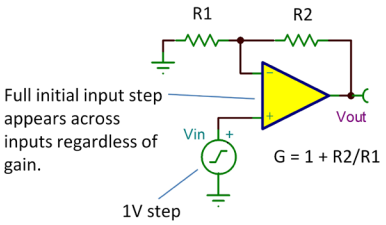
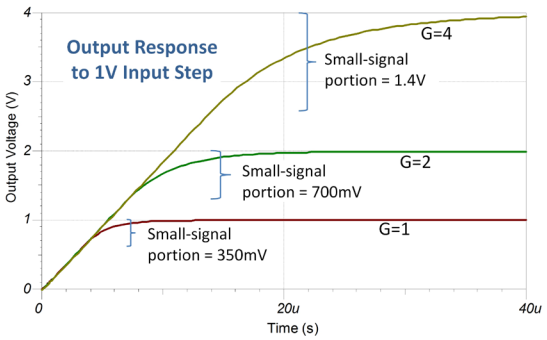


Figure 52: The slew rate is the same for any closed-loop gain but the onset of slewing is more gradual and occurs at higher output voltage in higher gains.



21. Settling time: a look at the character of the settling waveform

Settling time is the time required for an operational amplifier (op amp) to respond to an input-voltage step and then enter and stay within a specified error range of the final value. It is important in applications that drive an analog-to-digital converter (ADC), digitizing rapidly changing inputs. But let us look beyond the definition and focus on the character of settling waveforms.

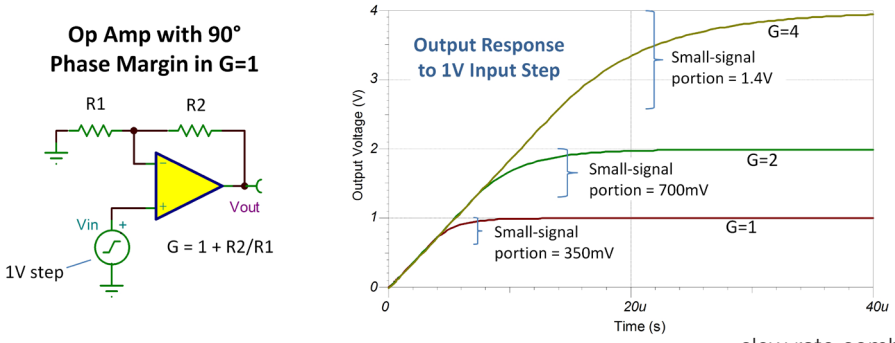


Figure 53: As closed-loop gain is increased, bandwidth is reduced and response is slower.

In section 20, I showed how an op amp transitions from a slewing ramp to a small-signal settling portion of the waveform; see **Figure 53**. As the gain increases, you can see the slower closure to final value.

This is due to reduced closed-loop bandwidth in higher gain. This example op amp is tuned to have virtually 90 degrees phase margin in G = 1. Notice that there is no overshoot, even in unity gain. Its virtually perfect first-order response serves as a benchmark for comparison, but you are unlikely to find an op amp with such generous phase margin in G = 1.

The response in **Figure 54** is more realistic (maybe a bit pessimistic). These waveforms are produced by the same op amp but with an approximately 35 degrees phase margin at G = 1. (The ideal op amp responses are also shown for comparison.) Its small-signal overshoot is approximately 32 percent in G = 1. It appears to be less overshoot with the 1-V step shown because only the small-signal portion of the response produces this overshoot behavior. A larger input step would have the same magnitude overshoot but look proportionally even smaller. That is why you should always check overshoot and stability with small input-voltage steps.

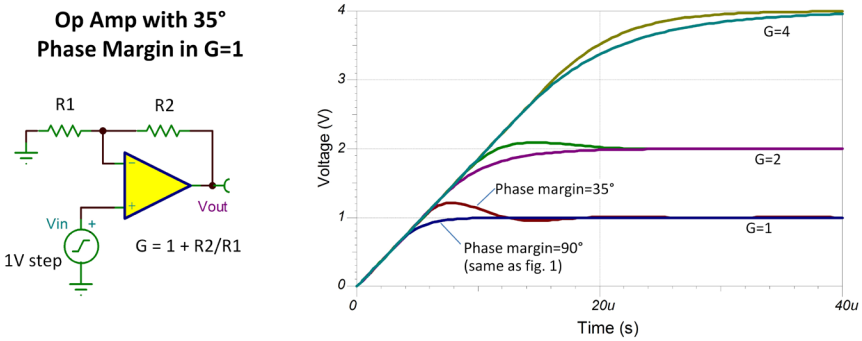


Figure 54: Waveforms produced by the same op amp, but with approximately 35° phase margin at G = 1.

Figure 55 shows an expanded view of the G = 1 small-signal response. Note that the settling of the final humps to a final steady value appear to require two complete up/down cycles. The wiggles continue, smaller and smaller – beyond the resolution of this graph. An additional cycle or two might be required to settle to high accuracy.

When you visualize this final settling behavior, you may imagine a compressed time scale in the final over/undershoots, as if the natural frequency of this ringing is shifting upward with each hump. But every cycle of settling requires the same time. Excessive ringing can be costly – a good reason to select a reasonably well-behaved op amp.

The true settling time to high accuracy (16 bits or greater) often includes other factors. Behaviors produced by fancier phase-compensation techniques and thermal effects can add to the settling time. The amplifier can also be perturbed by glitches from the input switching of an ADC. Optimizing all this can be tricky business. Still, it is important to visualize the primary effects at work – slew rate combined with a second-order system response.

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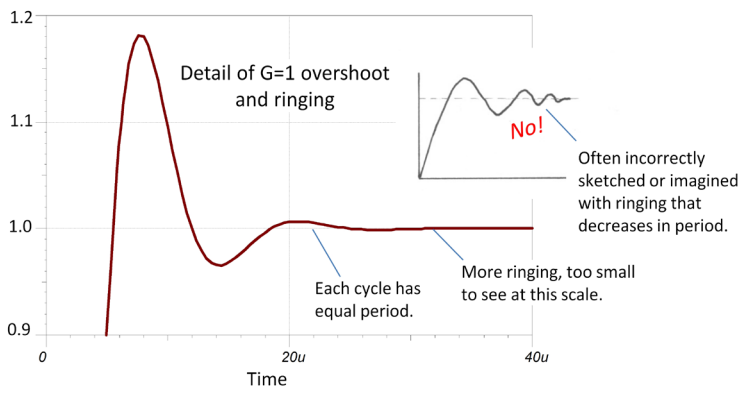

Figure 55: An expanded view of a G = 1 small-signal showing that the period of ringing is constant.

22. Resistor noise: reviewing basics, plus a fun quiz

The noise performance of amplifier circuits is greatly affected by the Johnson noise of resistors: the source resistance and feedback resistors. Most everyone seems to know that resistors have noise but may be a bit foggy on some of the details. Here is a bite-sized review in preparation for future discussions on amplifier noise.

The Thevenin noise model for a resistor consists of a noiseless resistor in series with a noise voltage; see **Figure 56**.

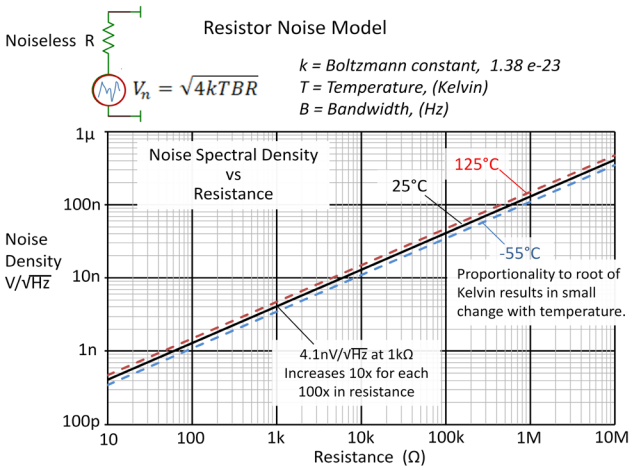

Figure 56: A resistor's Thevenin noise model is a noiseless resistor in series with a noise voltage.

The noise voltage is proportional to the root of the resistance, bandwidth and temperature (Kelvin). TI often quantifies the noise in a 1-Hz bandwidth as its spectral density. The theoretical noise of a resistor is "white," meaning that it is spread uniformly over frequency. It has equal noise voltage in every equal slice of bandwidth.

The noise in each 1-Hz band sums randomly according to the root of the sum of the squares. We often refer to the spectral density in volts/root-Hertz. The numerical value is the same as for a 1-Hz bandwidth. For white noise, it is convenient to multiply by the square root of a bandwidth to sum the random contribution of each 1-Hz band. To measure or quantify the total noise, you need to limit the bandwidth (**Figure 57**). Without a known cutoff frequency, you do not know how much noise you are integrating.

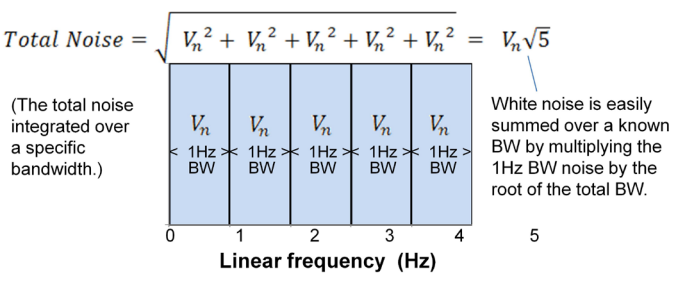

Figure 57: Summing the incremental 1-Hz bandwidths of white noise.

You may instinctively think of spectral plots as having a logarithmic frequency axis – a Bode plot. Note that a Bode plot has more hertz of bandwidth on the right side than the left side. Considering total noise, the right side of a Bode plot may be much more important than the left side.

Resistor noise is also Gaussian, a description of its amplitude distribution, a probability density function. It is Gaussian because it was created by the summation of a gazillion little random events. The central limit theorem explains how this noise becomes Gaussian. The root-mean-square (RMS) voltage of alternating current (AC) noise is equal to ±1 σ of the amplitude distribution (**Figure 58**). For 1-V RMS noise, there is a 68 percent (±1-σ) probability that the instantaneous voltage will be within a ±1-V range. A common misconception is to relate or equate white and Gaussian, but they are unrelated. Filtered resistor noise, for example, is not white but remains Gaussian. Binary noise is definitely not Gaussian, but it can be white. Resistor noise is white **and** Gaussian.

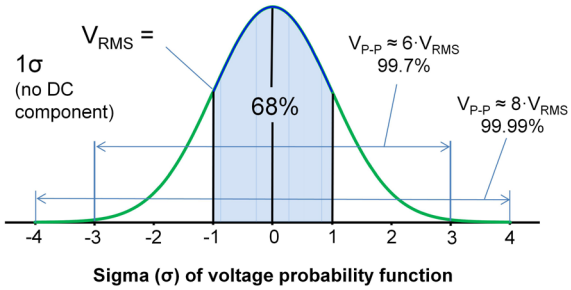

Figure 58: Gaussian noise spikes outside the ±3-times range are rare.

Purists like to rant that Gaussian noise does not have a defined peak-to-peak value – it is infinite, they say. True enough – the tails of a Gaussian distribution reach to infinity, so any voltage is possible. As a practical matter, the likelihood of noise spikes beyond ±3 times the RMS value is pretty small. Many folks use an approximation of six times the RMS for the peak-to-peak value. You can add a large additional guardband by using eight times the RMS without greatly changing the value.

Some fun points to ponder: The noise voltages of two resistors in series sum randomly, and the result is the same noise as for the sum of the resistor values. Similarly, the noise of resistors in parallel results in the noise of the parallel resistance. If it worked out differently, it would be problematic: think about bisecting a physical resistor and combining them in series or parallel. But it all works out.

A large-value resistor lying on your desk will not arc and spark from unlimited self-generated noise voltage. Stray parallel capacitance will limit the bandwidth and the total voltage. Similarly, the high-noise voltage you might imagine on insulators is shunted by parallel capacitance and the resistance of conductors around them.

Fun quiz: What is the total open-circuit noise voltage on a resistor that has a stray parallel capacitance of 0.5 pF? The solution details are here.

To see this original post with comments, click here.

23. Op amp noise: the noninverting amplifier

Building on the discussion of resistor noise in section 22, let us check out some basics of amplifier noise. The noninverting operational amplifier (op amp) configuration is most common for low-noise applications, so I will make that the focus.

Modeling the input source as a voltage noise source with a series resistance (**Figure 59**), you know that the source resistance, R_S, has a noise proportional to the root of its resistance (the straight line in **Figure 60**). The goal of a low-noise amplifier is to contribute minimal additional noise to what the source resistance generates.

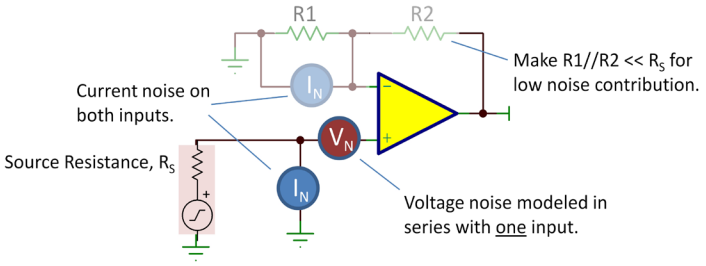

Figure 59: Amplifier noise is modeled as a voltage noise in series with one input and current noise sources connected to each input.

The amplifier noise is modeled as a voltage noise in series with one input and current-noise sources connected to each input; see **Figure 59**. Think of the voltage noise as just a time-varying component of offset voltage. Likewise, the current noise is a time-varying component of input bias current, one on each input. Ignore the current noise at the inverting input in this circuit – you can usually make its noise contribution minimal.

Figure 60 shows the total input-referred noise of the circuit for two op amps – the bipolar junction transistor (BJT)-input OPA209 and the junction FET (JFET)-input OPA140. Each is shown relative to the noise of the source resistance at 25°C. The three sources of noise are summed by root sum of squares for each op amp. You may have seen this graph in some op amp datasheets.

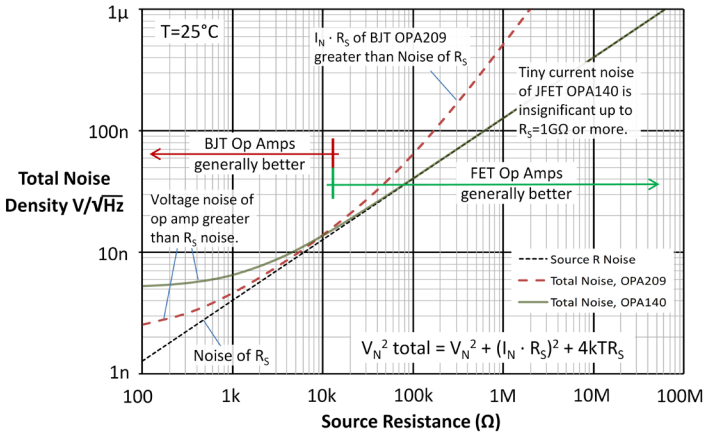

Figure 60: Using the OPA209, voltage noise dominates at low source resistance and current noise dominates at high source resistance.

As the source resistance decreases, its attendant Johnson noise decreases (by the inverse of the root of the resistance), and at some point the amplifier's voltage noise dominates. The total noise flattens to a value equal to the voltage noise of the amplifier. As the source resistance increases, the current noise flowing through the source resistance creates noise that increases linearly, rising more rapidly and eventually exceeding the noise of the source resistor. So, with high source resistance, the current noise effects dominate.

The greatest challenges in a low-noise amplifier design often come with low source resistance – 2 kΩ and lower. The lower source-resistance noise in this region demands amplifiers with very low-voltage noise. In general, BJT-input amplifiers excel in this range. Notice also that the total noise of the OPA209 in **Figure 60** dips nearest to that of the source resistance at a "sweet spot." This source resistance of best noise performance occurs at $R_S = V_N/I_N$.

FET-input amplifiers contribute little additional noise, with source resistance above 20 kΩ or so. The current noise of a FET op amp does not generally play an important role until you reach multigigaohm source resistance. A guideline: Below 10-kΩ source resistance, low-noise BJT amplifiers generally provide lower noise. Above approximately 10 kΩ, FET or complementary metal-oxide semiconductor (CMOS) op amps will likely have an advantage.

The feedback network, R1 and R2, also contributes noise but you can generally make this insignificant. How? The short answer is that if the parallel combination of R1 and R2 is one-tenth of R_S (or less), they will add less than 10 percent (<1 dB) to the total noise. This is true regardless of the ratio of the resistors that set the closed-loop gain. The noise of feedback components is assumed to be zero in **Figure 60**.

Of course, there is much more to know, but an understanding of this frequent case is a good start. Want more? I recommend "Operational Amplifier Noise: Techniques and Tips for Analyzing and Reducing Noise," written by my colleague Art Kay.

Point to ponder: The OPA140 has a very broad resistance range above 10 kΩ where noise performance is excellent. Is there a way to adapt a lower source resistance to take advantage of this region of operation?

To see this original post with comments, click here.

24. Op amp noise: but what about the feedback resistors?

In section 23 I explored noninverting amplifier noise, but I dodged the issue of the feedback network's noise contribution. So what about the noise from R1 and R2 in **Figure 61**?

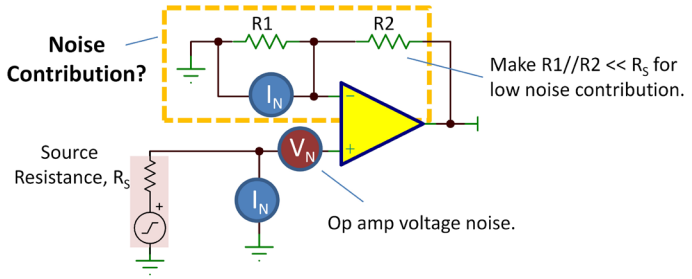

Figure 61: The inverting input comprises the feedback resistors' thermal noise and the op amp's current noise reacting with R1 and R2 components.

The noise contribution at the inverting input comprises the thermal noise of the feedback resistors and the operational amplifier's (op amp's) current noise reacting with R1 and R2 components. You can calculate the output contribution of these noise sources using basic op amp assumptions:

- R1's thermal-noise voltage is amplified to the output by the inverting gain of the circuit, –R2/R1.
- R2's thermal noise contributes directly to the output noise.
- The inverting input current noise flows through R2, resulting in an output noise contribution of $I_N \times R2$.

These noise sources are uncorrelated, so they "add" by the root sum of the squares.

But there is a more intuitive way to look at this. It can be handy to refer to noise sources as if they all occur at the noninverting input. Output noise contributions are divided by the noninverting gain. This referred-to-input (RTI) approach makes it easy to compare noise sources to the input signal.

The noise occurring at the inverting input relates to the parallel combination of R1 and R2. When referred to the noninverting input, the combined RTI thermal noise of R1 and R2 is equal to the thermal noise of R1//R2. The current-noise RTI contribution at the inverting input is equal to $I_N \times (R1//R2)$. It is all about R1//R2.

Noise contribution of R1 and R2 and inverting current noise (equation 2):

$$\text{Output Noise}^2 = [\, V_{NR1} \cdot (R2/R1)\,]^2 + (V_{NR2})^2 + (\, I_N \cdot R2\,)^2 \quad (2)$$

Dividing by non-inverting gain to refer to input (equation 3):

$$\text{RTI Noise}^2 = (V_{NR1//R2})^2 + (\, I_N \cdot R1//R2\,)^2 \quad (3)$$

Thermal noise of R1//R2

This result reveals an important factor for a low-noise design. Make $R1//R2 < R_S$ and the noise contribution at the inverting input is negligible. If $R1//R2 = R_S$, then the feedback network contributes equal noise to that of the source resistance. That may be too much for some designs.

In high gains, it is easy to keep the parallel resistance low – R1 can be made much less than Rs and R2 is big. At moderate gains it gets more difficult. G = 2 is the worst case when R1 and R2 are equal. If you want to make the parallel resistance 100 Ω, for example, R1 and R2 need to be 200 Ω.

The feedback network then imposes a 400-Ω load on the op amp – too low in most circumstances. It gets easy again very close to G = 1 when R1 is big and R2 is small. This case is not common because you generally want significant gain in the first low-noise stage.

To address a common concern: There is no inherent noise penalty in making R2 a high resistance. If you can achieve higher gain by increasing R2 and decreasing R1 while maintaining a constant parallel resistance, noise performance remains constant.

You can download an Excel file to calculate the noise of this commonly used input-amplifier stage, including the op amp and source-resistance noise. It shows the percentage contribution of each noise source and graphs the total noise over a range of source resistance. It also calculates noise figure, which is the noise (in decibels) that the amplifier adds to thermal noise of the source. This is a handy measure of the noise performance of the amplifier. Tinker with it and you will quickly get a feel for the issues and trade-offs.

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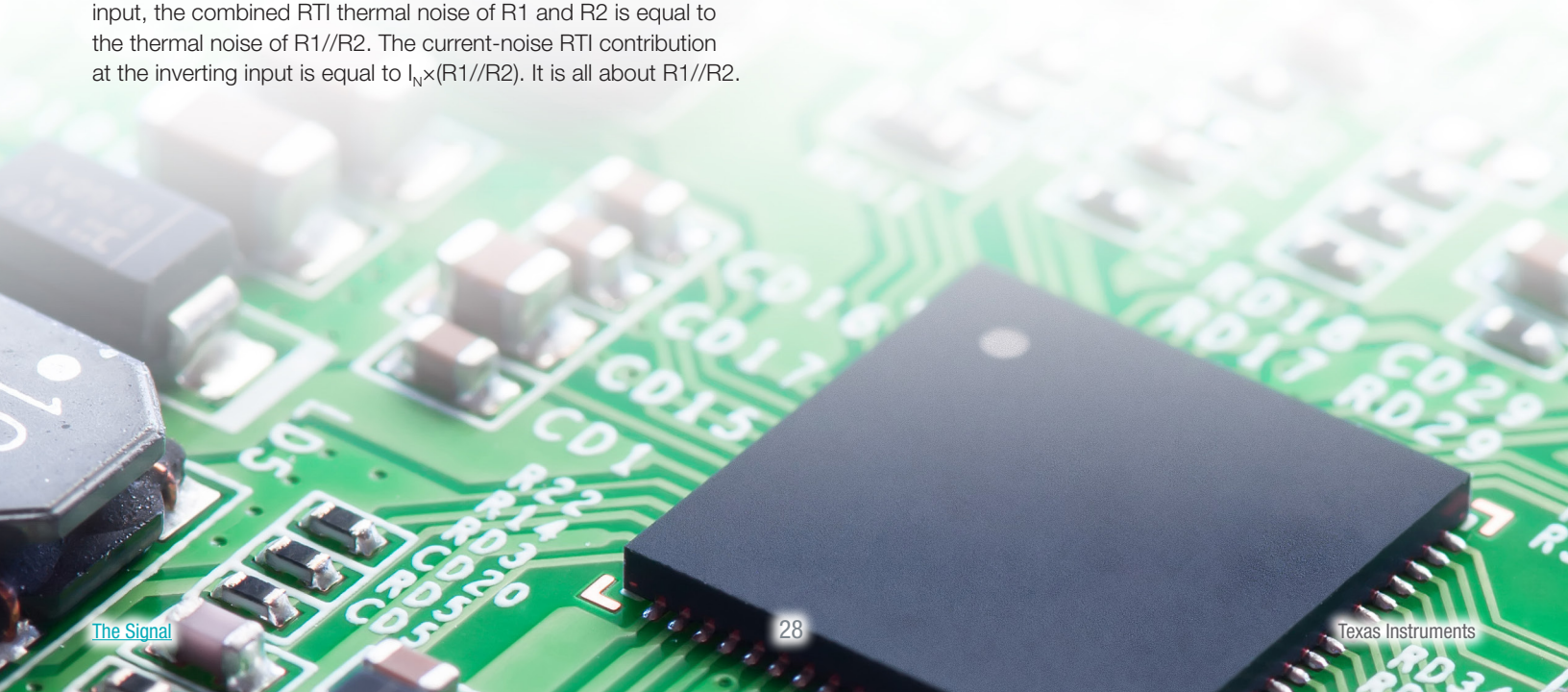

25. 1/f noise: the flickering candle

The one-over-f (1/f) low-frequency noise region of amplifiers seems just a bit mysterious. It is also called flicker noise, like a flickering candle. Seen on an oscilloscope with a slow sweep, it has a wandering baseline (**Figure 62**) because the high-frequency noise rides on larger low-frequency content. Pink noise, another metaphoric name, also suggests a stronger low-frequency component. Flicker noise seems ever-present in physical systems and life science. Weather/climate patterns, for example, have a 1/f component. I will not attempt to explain why it is found in semiconductors – deep subject!

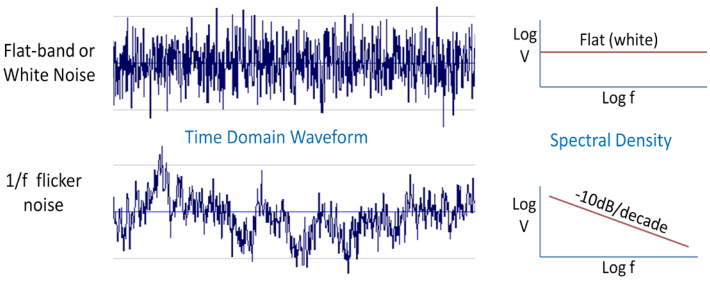

Figure 62: White noise (top) compared with 1/f noise (bottom).

The spectrum of flicker noise has a nominal slope of -10 dB/decade, half that of a single resistor-capacitor (RC) pole. Note that it's the square of the voltage (or power) that declines at a 1/f rate. Noise voltage falls at 1/sqrt(f). The actual slope can vary somewhat, but this does not greatly change its behavior or the conclusions.

A measured spectrum of flicker noise generally looks lumpy, with dips and valleys. You need to average for long periods to get a reasonably smooth plot. The period of 0.1-Hz noise content is 10 seconds, so for a good measurement down to 0.1 Hz you need to average many 10-second periods – five minutes or more. For 0.01-Hz data, take a long lunch. If you repeat the measurement it will likely look different. Noise is noisy and 1/f noise seems noisier than most other noise (did I write that?).

To calculate total noise, V_B, over a bandwidth (f_1 to f_2), integrate the 1/f function which results in the natural logarithm of the frequency ratio, f_2/f_1.

(4)

$$V_B^2 = v_a^2 f_a \int_{f1}^{f2} \frac{1}{f}\, df = v_a^2 f_a \cdot ln\left(\frac{f_2}{f_1}\right); \quad V_B = v_a \sqrt{f_a \cdot ln\left(\frac{f_2}{f_1}\right)}$$

Where v_a is the flicker spot noise density at frequency f_a.

Points to ponder:

- Each decade of frequency (or other constant ratio of frequencies) contributes equally to total noise. Each successive decade has lower noise density but more bandwidth.
- From the spectral plot, you might infer that 1/f noise grows boundlessly as you measure for increasingly long periods. It does, but very slowly. Noise from 0.1 to 10 Hz doubles (approximately) with a lower bandwidth extended to 3.17e-8 Hz (a one-year period). Add another six percent for 10 years.
- It is challenging, but not impossible, to filter 1/f noise. Flicker noise from 0.1 Hz to 1 kHz (four decades) filtered to 10 Hz (two decades) only reduces the noise by 3 dB. Resistor values must be low for low noise, which makes capacitor values large for a low-frequency cutoff.

Amplifier noise is a combination of 1/f noise and flat (white) noise. The flat noise continues at a low frequency but 1/f noise dominates (**Figure 63**). The 1/f noise continues at a high frequency but flat noise dominates. The two blend at the corner frequency, adding randomly to make a 3-dB increase.

Amplifier noise is summed over the f_1 to f_2 bandwidth by integrating the 1/f and flat noise separately over the bandwidth, and then combined by the root sum of squares.

Other points to ponder are:

- An N-times increase in flicker-noise density increases the corner frequency by N^2.
- The total noise from a decade below to a decade above the corner frequency is dominated by the flat-band noise (68 percent) even though the 1/f noise region "looks bigger."

You can download an Excel file here that calculates integrated 1/f noise and flat-band noise, producing a graph and data similar to **Figure 63**. Tinker with it to get a better feel for the issues.

Amplifiers with bipolar junction transistor (BJT)-input stages (OPA211) generally have lower 1/f noise, but new-generation analog integrated circuit (IC) processes have greatly improved junction FET (JFET) and complementary metal-oxide semiconductor (CMOS) transistors. The OPA140 (JFET) and OPA376 (CMOS) operational amplifiers, for example, have corner frequencies of 10 Hz and 50 Hz, respectively. Chopper amplifiers virtually eliminate 1/f noise by correcting offset-voltage changes.

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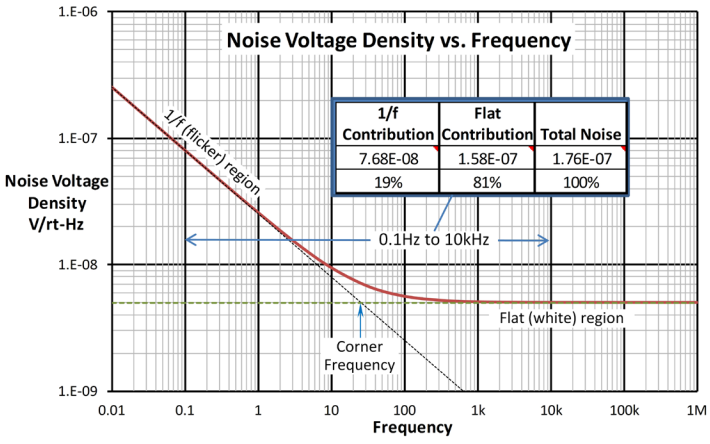


Figure 63: Amplifier noise in this graph is a combination of 1/f noise and flat (white) noise.

26. Chopper op amps: are they really noisy?

Chopper operational amplifiers (op amps) offer very low offset voltage and dramatically reduce low-frequency 1/f (flicker) noise. How do they do it?

Figure 64 shows the input stage of a chopper op amp. The amplifier is a relatively conventional transconductance stage with differential input and differential output current. Chopping is accomplished with commutating switches on the input and output that synchronously reverse the polarity. Since both differential input and output are reversed simultaneously, the net effect on the output capacitor, C1, is a constant signal-path polarity.

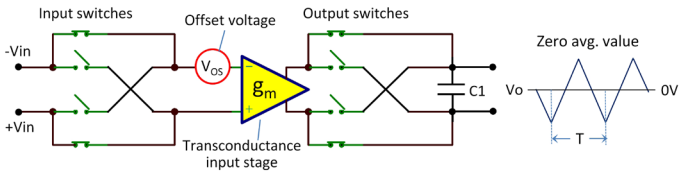


Figure 64: Input stage of a chopper op amp.

The offset voltage of the transconductance stage is inside the input switching network, so its contribution to output is periodically reversed by the output switches. The output current caused by offset voltage causes the voltage on C1 to ramp up and down at an equal rate. Internal logic assures equal up and down ramp times, so the average output voltage on C1 is zero. Thus, zero offset!

Early-generation choppers provided only modest filtering of triangular chopping noise, causing them to be branded as wickedly noisy devices, used only when very low offset voltage was crucial. (And this is how big, noisy motorcycles came to be.) Particularly troublesome was that the pre-chopping offset voltage determined the magnitude of the triangle waveform, so chopping noise could vary considerably from unit to unit.

New-generation choppers are dramatically quieter, incorporating a switched-capacitor filter with multiple notches aligned with the chopping frequency and its odd harmonics. This is accomplished by integrating a charge on C1 for a full cycle before transferring its charge to the next stage of the op amp. Integrated over a full up-down cycle, its net value is zero – perfectly averaged. In the frequency domain, this creates a sinc(x) or sin(x)/x filter response with nulls that precisely align with the fundamental and all harmonics of the triangle wave (**Figure 65**).

In its final implementation, eight switches in the output-commutation network alternately charge two C1 capacitors. This enables integration of the input signal on one capacitor, while charge on the other capacitor transfers to the next stage of the op amp.

Since 1/f (flicker) noise is merely a slow time-varying offset voltage, choppers virtually eliminate this increased noise-spectral density in the low-frequency range. The chopping shifts the baseband signal to the chopping frequency, beyond the input stage's 1/f region. Thus, the low-frequency signal range of the chopper has a noise-spectral density equal to that of the amplifier's high-frequency range.

I made this all sound neat and tidy. Zero offset ... perfect! Of course, there is still some residual offset error produced by switching charge injection and the mismatch of capacitance and parasitics. The gain of the input stage (discussed here) greatly reduces offset contributed by later op amp stages. In general, a wider amplifier bandwidth requires faster chopping, which increases residual offset errors. The residual offset tends to be very stable with temperature and through product life, an important attribute for these devices.

Now I do not claim that modern chopper op amps eliminate the need for standard op amps: far from it. But new-generation choppers are now useful in a much wider range of applications. They provide very low and stable offset voltage, virtually no flicker noise, and very near the behavior of a standard op amp.

To see this original post with comments, click here.

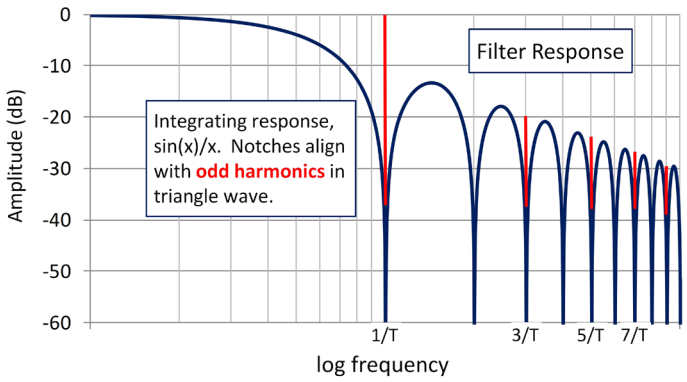
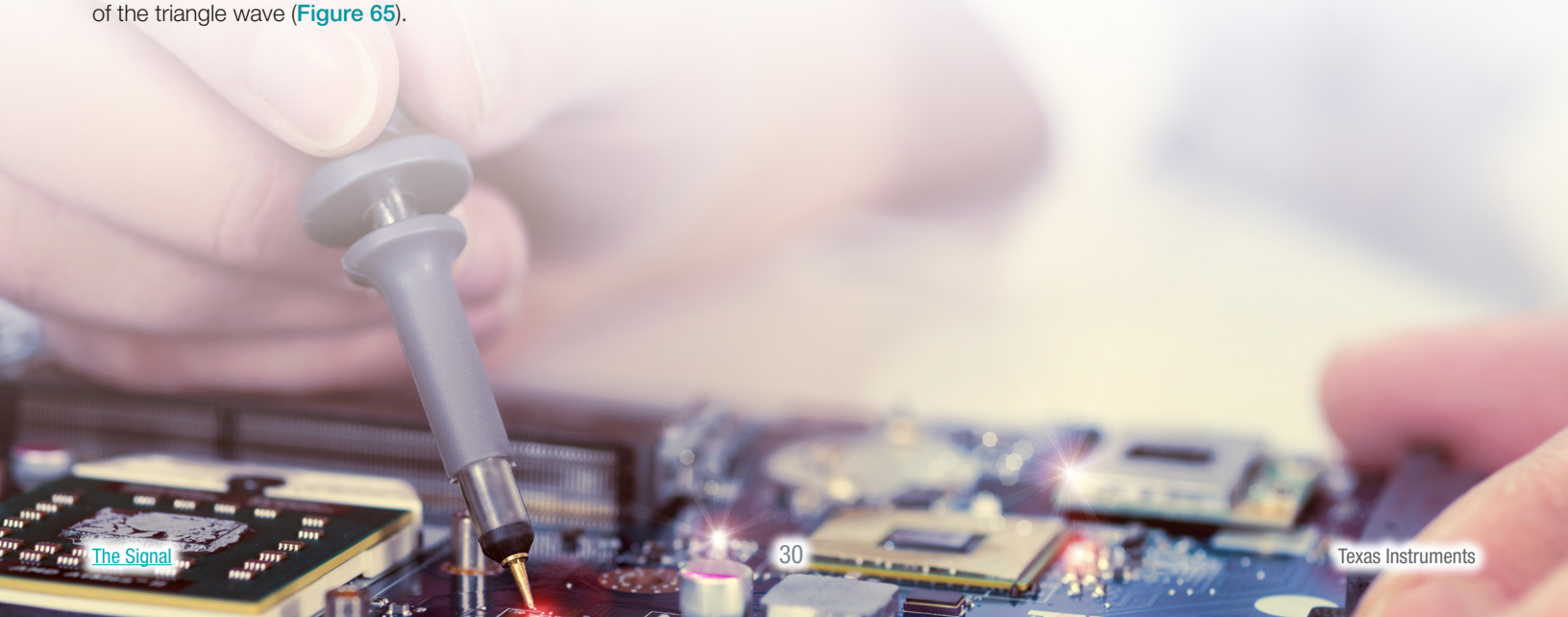


Figure 65: New-generation chopper op amps incorporate a switched-capacitor filter with multiple notches aligned with the chopping frequency and its harmonics.



27. Bypass capacitors: yes they are needed, but why?

Everyone knows that op amps should have power supply bypass capacitors located near the IC's terminals, right? But why? Why, for example, is an amplifier more apt to oscillate without proper bypassing? The reasons will increase your understanding and awareness.

Power supply rejection is an amplifier's ability to reject variations in the power supply voltage. **Figure 66**, for example, shows that this rejection capability is very good at low frequency, but diminishes as frequency increases. So there is poorer rejection at high frequency where oscillations occur.

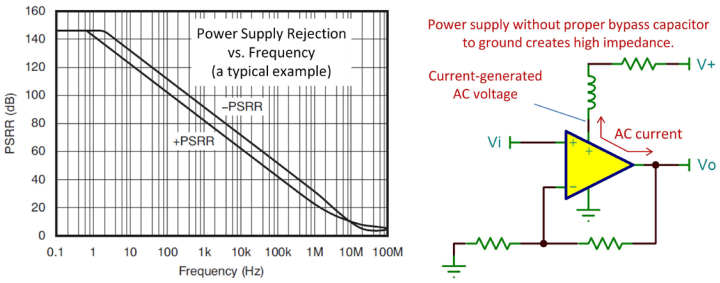


Figure 66: Power supply without proper bypass capacitor to ground creates high impedance.

We often think of external power supply-borne noise interfering with an amplifier. But op amps can create their own problems. For example, output load current must come from the power supply terminals. Without proper bypassing the impedance at a supply terminal can be high. This allows alternating current (AC) load current to produce an AC voltage on the supply pin. This creates an unintended, uncontrolled feedback path. Inductance in this power supply connection can magnify the resulting AC voltage at the supply pin. At high frequency, where power supply rejection is poor, this unintended feedback can cause oscillation.

There are internal forces at work, too. Without a solid power supply, internal circuit nodes may talk to one another, creating unwanted feedback paths. Internal circuitry is designed to operate with firm, low impedance on the power supply terminals. An amplifier may behave quite differently and unpredictably without the solid base of low-impedance supplies.

With a clean sine wave input, the unintended feedback due to poor bypassing may not be a tidy sine wave. The signal currents in the supply terminals, **Figure 67**, are often highly distorted because they only represent half of sine wave current. With different power supply rejection characteristics on the positive and negative supplies, the net effect will distort the output waveform.

The issues are magnified with high load current. Reactive loads create phase-shifted load currents that may exacerbate issues. Capacitive loads are already at higher risk of oscillations due to additional phase shift in the feedback path. These higher risk cases may need higher value tantalum bypass capacitors and extra care in circuit layout, compact and direct.

Of course, not all poorly bypassed amplifiers oscillate. There may not be sufficient positive feedback, or the phase not quite right (or wrong!) to sustain an oscillation. Nevertheless, performance may be compromised. Frequency and pulse response may be affected with excessive overshoot and poor settling time. These behaviors are not well-modeled in TINA-TI or other simulation program with integrated circuit emphasis (SPICE). Voltage sources in SPICE are perfectly solid, unperturbed by load currents. Modeling the actual source impedance of your supply and board layout with additional components is tricky and imprecise. Power supply rejection magnitude is modeled in our best macro-models, but the phase relationship of this feedback path is unlikely to match reality. Simulation can be tremendously useful, but won't accurately predict this behavior.

All this should not cause you to be paranoid – no need to go crazy with bypassing. Just be alert to particularly sensitive situations and signs of potential problems. Good analog design thrives with a healthy dose of understanding and awareness.

To see this original post with comments, click here.

Figure 67: Positive and negative power supply current waveforms are often highly distorted because they only represent half of sine wave current (right).

28. The unused op amp: what to do?

When I talk about unused op amps, I am not referring to op amps in your parts bin. Those should be in anti-static bags or conductive foam. What about the one on your circuit board—the unused op amp in a quad- or dual-package?

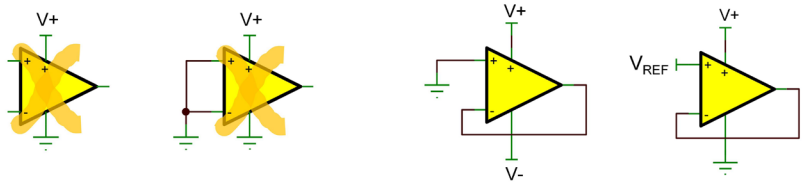
It is best to connect the op amp in a real op amp circuit with feedback (**Figure 68**). A unity-gain buffer is an obvious choice since no additional components are required (right image). Then connect the input to a voltage within its linear input and output range. Connections (or open-circuit inputs) that can potentially overload the input, output, or leave the amplifier in an indeterminate noisy state are undesirable (left image).

A suggestion on circuit board layout: position any unused op amps for possible future modifications. You may find a use for a spare op amp in a redesign or future product spin. Think ahead. Make the connections to the spare op amp on top and bottom circuit board layers where minor surgery can easily test your changes. You might even provide layout positions for feedback components with traces to tie-off nodes that can be easily cut.

You can avoid all of these issues completely by selecting an amplifier type that has single, dual and quad versions – the OPA322 is one example. This can allow an optimized circuit board layout with no orphans while using op amps with the same specs and behavior.

A word of comfort to those who may not have used a preferred method to tie-off an unused amplifier: you are unlikely to greatly disturb the working op amp(s) in the same package. While you may be drawing some extra current in the unused amp, your system is unlikely to crash and burn. Most modern op amps have independent biasing circuitry, unperturbed by overloads in other channels on the same chip. If your circuits are working, relax and follow best practices in your next design.

To see this original post with comments, click here.



Floating inputs or both inputs connected to the same node will usually cause the output to saturate to a supply rail and can cause increased quiescent current. Floating inputs may also pick up capacitively coupled noise.

With ± supplies, a G = 1 follower with input grounded input is generally very safe. With a single supply, connect the input to a node within linear I/O range. A reference voltage or other low-impedance node may serve the purpose.

Figure 68: Connecting an unused op amp: the wrong way (left) and the right way (right).

29. Protecting inputs from EOS damage EOS over-voltage

When providing a sensitive amplifier input terminal to the outside world, designers wonder what someone might connect it to or how it might be treated. Will it be treated with care, or could they carelessly plug it into the alternating current (AC) mains? We all would like to make our equipment robust, able to sustain the most brutal treatment, so I will explain how to protect against electrical over-stress (EOS).

The OPA320 is typical of most op amps. The absolute maximum ratings describe the maximum power supply voltage, and the maximum input terminal voltage and current (**Figure 69**). The accompanying note indicates that if you limit input current, you do not need to limit the input voltage. Internal clamp diodes are safe to ±10 mA. However, limiting the current with high-voltage overloads can require a high series input resistance, increasing noise, decreasing bandwidth and possibly creating other errors.

ABSOLUTE MAXIMUM RATINGS **OPA320**

Supply voltage, V- to V+		6V
Signal input pins	Voltage	(V-) - 0.5 to (V+) + 0.5V
	Current	±10 mA

Input terminals are diode-clamped to the power supply rails. Input signals that can swing more than 0.5 V beyond the rails should be limited to 10 mA or less.

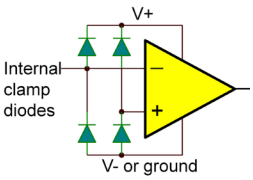


Figure 69: Example of an op amp with absolute maximum ratings for power supply voltage and input terminal voltage and current. Internal input clamp diodes shown (right).

The clamp diodes begin conducting when the input voltage exceeds the rails by 0.6 V or so. Many devices can typically tolerate higher current, but the forward voltages increases dramatically – increasing the chance of damage.

You can greatly improve tolerance to higher fault currents and increase the level of protection by adding external diodes. Common signal diodes, such as the ubiquitous 1N4148, typically have a significantly lower forward voltage than the internal clamp diodes.

In bench tests, I found that a variety of 1N4148 diodes in our bin all had forward voltages that are at least 100 mV lower than the internal clamps on our amplifiers. Connected in parallel with the internal ones, the majority of the fault current will flow in the external diode.

Schottky diodes have an even lower forward voltage and may provide improved protection. The disadvantage is that they tend to be very leaky. Reverse leakage current specifications are generally a microamp or more, and that is at room temperature. Leakage rises with temperature.

Beware … you need a solid power supply voltage. Clamp diodes, whether internal or external, rely on a relatively steady power supply voltage to limit the stress. If the offending fault pulse can dump enough current into the power supply rail, raising (or lowering, on V–) the power supply, it can overstress the supply voltage terminal (**Figure 70**). A typical positive linear regulator cannot sink current and cannot be relied upon to hold a steady voltage. Larger supply bypass capacitors can help absorb a large pulse of fault current. Sustained fault current may require a Zener clamp on the power supply. Use a Zener clamp just above the maximum power supply voltage so that it only conducts during a fault. Note that on ± supplies, you would need equivalent protection on the negative side.

These measures still may lead to voltages beyond the rated maximum values, but here is the point: absolute maximum ratings are generally very safe and damage at these voltages or current is extremely unlikely. There is generally a significant margin beyond these ratings where damage is still quite unlikely (but no promises). It is much easier to clamp to a couple volts beyond these ratings, and you are still likely to achieve high survival rate. In many cases, the goal is to dramatically improve the survival rate without great expense or performance compromises.

It is not possible to recommend a one-size-fits-all solution or assure that a particular protection scheme will meet your needs, because application details vary widely. Amplifiers differ in their sensitivity, and the needed level of protection differs dramatically. Sacrifice some amplifiers with some torture testing, if necessary.

To see this original post with comments, click here.

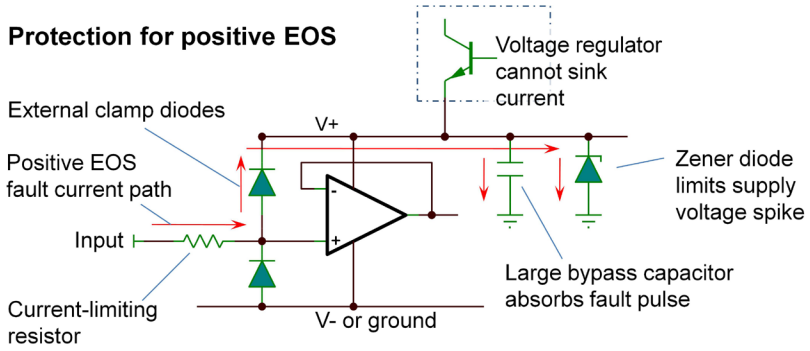


Figure 70: Input over-voltage can create excessive power supply voltage with conduction through the input protection diodes. A Zener diode limits the overstress.

30. Differential input clamps: can they affect your op amp circuits?

In one of my posts, I wrote about using operational amplifiers as a comparator, and we looked at the effect that internal differential input clamp diodes could have on these op amps. I posed the question, “Can these clamps affect op amp circuits?” Op amps should have near zero volts between the two input terminals, right? So these diodes will never forward bias in normal op amp circuits ... or will they?

In this discussion we will be talking about the differential clamp diodes that may be present in some op amps (**Figure 71**).

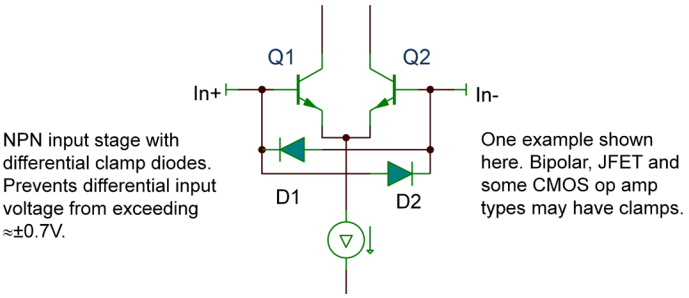


Figure 71: Many bipolor, JFET and some CMOS op amp types have internal differential clamp diodes.

The effect in op amp circuits is often seen in basic non-inverting amplifier configurations, including a simple G = 1 buffer amplifier. Consider a positive-going input step. The output cannot immediately follow the abrupt input voltage change. If the input step is greater than 0.7 V, D1 will conduct, disturbing the non-inverting input. During this period when the op amp is *slewing* to its new output voltage, the current in the input terminal of the op amp will spike to a much higher value (**Figure 72**). Eventually, when the output “catches up” to the input all will be well again.

Many applications process inherently slow or band-limited signals, well below the slew rate of the op amp so this behavior would never occur. In other applications, even with fast-changing input voltage, the transient in input terminal current does not adversely affect circuit operation. But in some special cases, the pulse of input current can cause problems. One noteworthy situation is in a multiplexed data acquisition system – a simplified case just showing two input channels is shown in **Figure 73**.

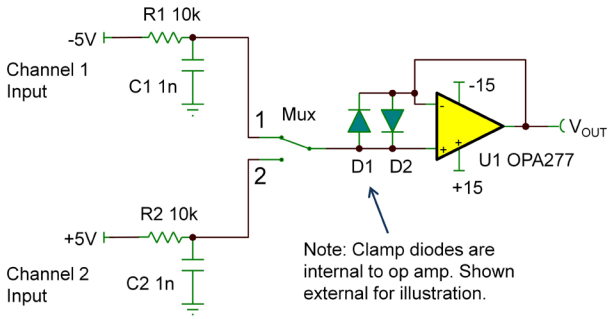


Figure 73: A multiplexed data acquisition system may suffer from errors if switching between channels creates input steps that can forward bias D1 or D2.

In this example, as the multiplexer switches from channel 1 to channel 2, U1’s output is required to quickly slew from –5 V to +5 V. D1 forward biases, and the resulting input current transient passes through the multiplexer switch, discharging the voltage on C2. R/C input filters are often used to hold a steady voltage during channel-switching, but the current pulse partially discharges C2. It now will take additional time for C2 to recharge to the correct input voltage; thus, slowing down the possible multiplex rate or reducing accuracy.

The solution is to use an op amp without differential clamps for U1. A FET-input amplifier, such as the OPA140, has low input bias current (so as to not load the series resistance of the MUX) and no differential input clamps. This is great for multiplexed inputs. The OPA827 is an extraordinary performer in most applications – FET input, very low noise, high speed and fast settling. But it has differential input clamps, so the OPA827 is probably not the best choice for the op amp following a multiplexer. A previous blog had some general guidelines on various op amp types with focus on differential clamps. Continue onto section 31 for more details.

I certainly don’t want to leave an impression that op amps with differential input clamps are risky and should be avoided – they are not. But with awareness, you can make better-informed selections in the rare instances where they could affect your circuits.

To see this original post with comments, click here.

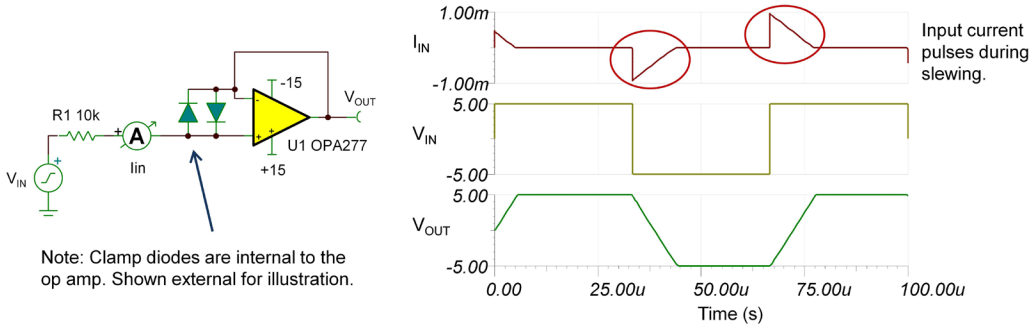


Figure 72: Internal input differential clamp diodes can create unexpected input current pulses with large input voltage steps.

31. Op amps used as comparators: is it okay?

Many of you (and I, too) occasionally use an operational amplifier (op amp) as a comparator. Often, this is when you only need one simple comparator and you have a "spare" op amp in a quad op amp package. The phase compensation required for a stable op amp operation means that it will be very slow as a comparator; however, if speed requirements are modest, the op amp may suffice. We get sporadic questions about this use of an op amp. While some op amps work okay, some don't operate as expected. Why?

Many op amps have voltage clamps between the input terminals, most often implemented with back-to-back diodes (sometimes with two or more diodes in series). These diodes protect the input transistors from reverse breakdown of their base-emitter junctions. With many IC processes, breakdown would occur at approximately 6-V differential input and could significantly alter or damage the transistor. With the negative-positive-negative (NPN) input stage shown in **Figure 74**, D1 and D2 provide the protection.

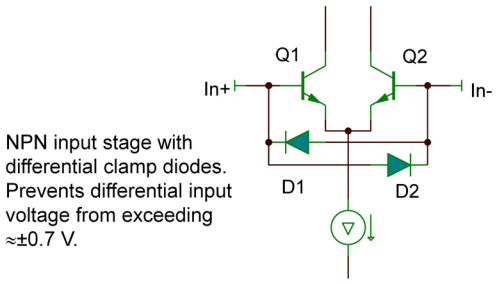


Figure 74: Internal differential clamp diodes in this op amp input stage prevent transistor damage but may create undesirable behavior when used as a comparator.

In most common op amp applications, you have near zero volts across the inputs and never turn on these diodes. But clearly, this protection can be a problem for comparator operation. You have a limited differential voltage range (0.7 V or so) before one input will tug on the other, pulling its voltage in an unexpected manner. This may not rule out its use as a comparator, but it would require some careful consideration. In some circuits, it may be totally unacceptable.

The problem is that TI and other op amp manufacturers have been inconsistent in communicating the presence of these clamps. Even when we do, we may not explain or interpret the message. Maybe we should say, "Be careful if used as a comparator!" The authors of datasheets often just assume that you are going to use an op amp as an op amp. We held a meeting with our team and resolved that we would communicate this more clearly in the future. But what about all the op amps already out there? Following are some guidelines that may help.

In general, op amps with bipolar NPN transistors have input clamps. Examples would be the OP07, OPA227, OPA277, and many others. An exception is the old µA741, which has NPN input transistors, but additional lateral positive-negative-positive (PNP) transistors in series that provided inherent protection for the NPNs (**Figure 75**).

General-purpose op amps with lateral PNP input transistors generally do not have input clamps. Examples include the LM324, LM358, OPA234, OPA2251 and the OPA244. These op amps are

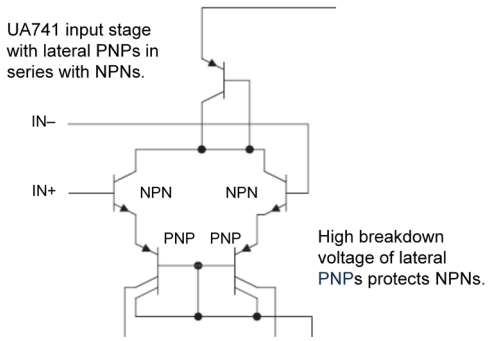


Figure 75: Some op amp input stage types use high breakdown voltage lateral PNPs that protect NPNs. These op amp types are better-suited to comparator operation.

generally "single-supply" types, meaning that they have a common-mode range that extends to the negative supply terminal or slightly below. They often can be identified because the input bias current is listed as a negative number, indicating that input bias current flows out of the input pins. Note, however, that high-speed op amps using PNP inputs generally have input clamps as these are vertical PNPs with lower breakdown voltage.

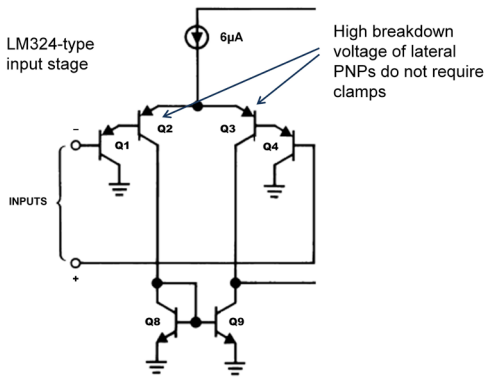


Figure 76: The LM324-type input stage uses high breakdown voltage lateral PNPs and does not require clamps. This op amp type is better-suited to comparator operation.

JFET and CMOS amplifiers that operate on higher voltage (greater than 20 V or so) may or may not have clamps. It is an iffy proposition that requires more checking. The characteristics of the process and the particular transistors used determine whether clamps are present internally.

Most low-voltage CMOS op amps do not have clamps. There is a special exception for auto-zero or chopper types that may have behaviors that look like clamps.

The bottom line ... if you consider using an op amp as a comparator, use caution. Glean what you can from the data sheet, including comments in the applications section. Validate its behavior in a breadboard or prototype, checking for influence of one input voltage on the other. Do not rely on a simulation program with integrated circuit emphasis (SPICE) macromodel. Some macromodels may not include extra components to model the clamps. Furthermore, other behaviors that can arise when you bang an op amp from rail to rail may not be accurately modeled.To see this original post with comments, click here.

More blog posts

If you want to read more from The Signal blog, below is a list of posts not included in this compendium.

Other amplifier issues

- Chopper op amps—are they really noisy?
- Differential input clamps—can they affect your op amp circuits?
- The unused op amp—what to do? (how to connect unused op amps)
- Typical—what does it mean in a datasheet specification?
- Matchy, Matchy—how alike are dual op amps?
- Bypass capacitors—yes, but why?
- Power supply bypassing—SPICE simulations vs. reality
- Put gain up front—waxing philosophical
- PCB layout tricks—striped capacitors and more
- Grounding principles (techniques for proper grounding and bypassing of amplifiers)

Protecting circuits ESD and EOS

- Protecting inputs from damage—EOS (protecting from input over-voltage)
- ESD—Zapp! (protecting circuits and systems from damage and functional failures)

Instrumentation and difference amplifiers

- Instrumentation amplifiers—avoiding a common pitfall
- Difference amplifiers—the need for well-matched resistors
- Making your own difference amp—sometimes 1% resistors are good enough

Application circuits and issues

- Handy gadgets and resistor divider calculations (a spreadsheet)
- Breadboarding with micro-packages—ouch!
- Current sources (and sinks)—understanding compliance range
- TIA Input Z: Infinite—or zero? What is it, really? (transimpedance amplifier input Z)
- Comparators—what's all the chatter?
- Paralleling op amps—is it possible?

Other components

- Op amps used as comparators—is it okay?
- Comparators—what's all the chatter? (hysteresis)
- Thermocouples—stuff that every analog designer should know
- Illuminating photodiodes (the basics)

Other components (cont.)

- When potentiometers go to pot (using pots in ratiometric mode)
- Controlling volume—log pots (volume controls)

Miscellany and fun

- Brain teaser—an infinite resistor network
- Brain teaser—the solution
- Resistor puzzle—the sequel
- Resistor puzzle solution—and a rant on good schematics
- Interview questions—memorable times on both sides
- Oh, that interview question— a reprise
- Pop quiz! (a 20-question quiz on various topics)
- Goop—a sticky topic
- Clairvoyant troubleshooting (using TI's E2E Community Forums)
- SPICE it up! … but does Bob Pease say no (is SPICE a crutch or a tool?)
- Honoring an analog giant (Remembering Bob Pease)

Additional resources

If you liked The Signal, here are more op amp resources you might find of interest:

- Watch training videos on topics such as input offset voltage and bias current, input and output limitations, power and temperature, bandwidth, slew rate and more in the TI Precision Labs – Op Amps training series.
- Put commonly used formulas at your fingertips with the Analog Engineer's Pocket Reference e-book. Topics include op amp bandwidth and stability, analog-to-digital and digital-to-analog conversions and more.

Get help with op amp product selection:

- Find your next op amp using TI's op amp quick search.
- Search for any suppliers' op amps to find similar TI devices by parameter with TI's op amp parametric cross-reference.

Answer to quiz on page 13:

Answer: These capacitors are made with a sandwich of two layers of metal foil separated by an insulating film layer, rolled into a cylindrical shape. They are non-polarized capacitors—the stripes are not polarity markings. The stripe identifies the terminal connected to the outside metal foil layer. The best orientation in a circuit depends on which terminal may be the more noise-sensitive node. See more on the subject at this blog: PCB layout tricks—striped capacitors and more….

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